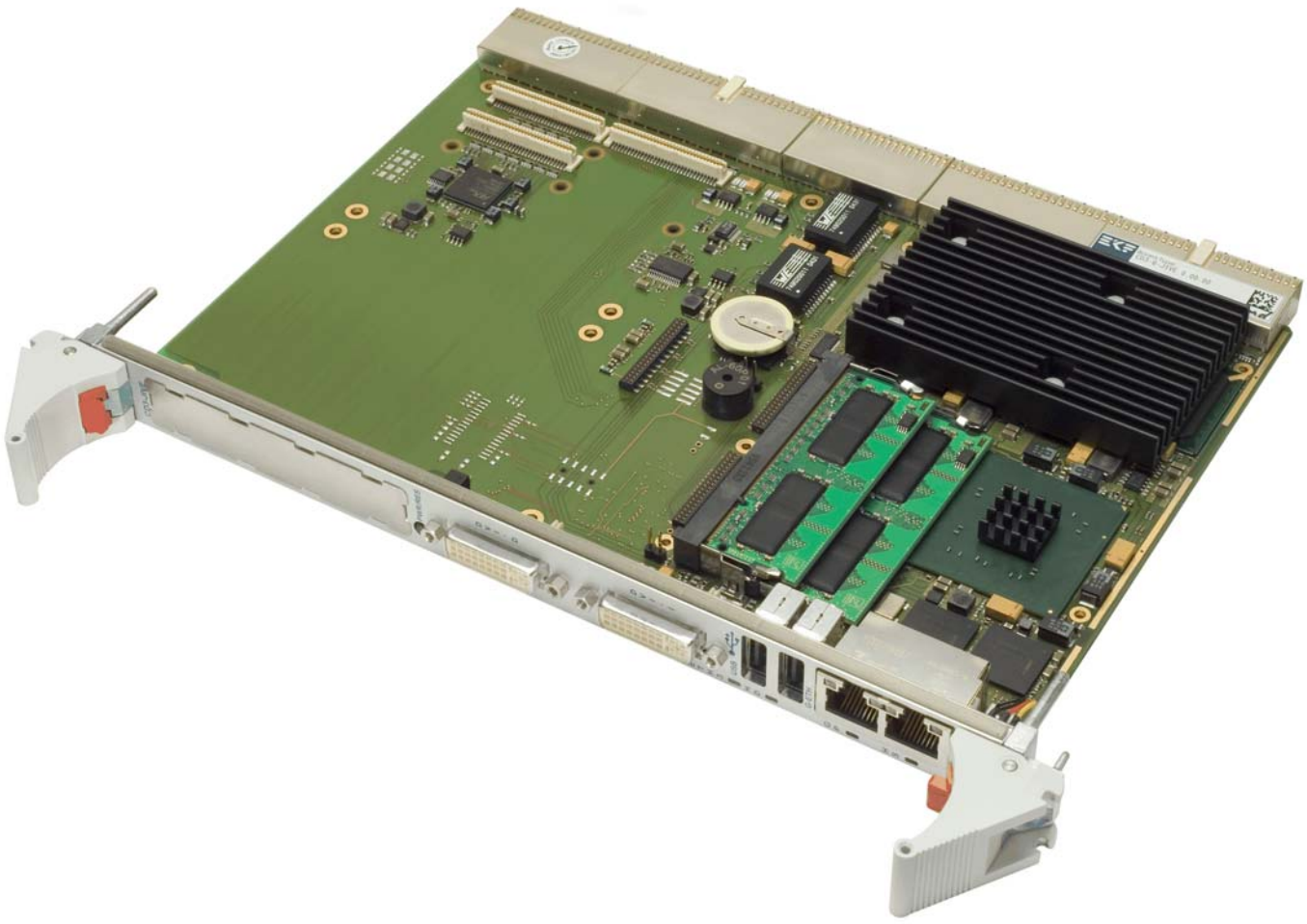
User Guide

CD3-JIVE • CompactPCI®

6U Advanced Pentium ® M CPU Board

Document No. 4197 • Edition 10

2010-09



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About this Manual

This manual describes the technical aspects of the CD3-JIVE, required for installation and system integration. It is intended for the experienced user only.

Edition History

Ed.	Contents/*Changes*	Author	Date
1	User Manual CD3-JIVE, english, initial edition (Text #4197, File: cd3_uge.wpd)	jb	2006-06-19
2	Review	jj	28 August 2006
3	Added additional Information Added photos CD3-JIVE, CDT-RIO, C14-SATA	jb	2007-02-02
4	Added +12V connectivity to table of expansion interface connector PEXP (pin 40) and to the table in section "Hardware Monitor LM87". Removed some typos.	jb	2007-06-05
5	Added additional Information Changed block diagram Added photos CD3-JIVE, C14-SATA with PMC	jb	2007-07-19
6	Added information regarding Ethernet Jumbo Frame support to table 'Feature Summary'	jj	7 February 2008
7	Added chapter serial COM port connector	jj	6 March 2008
8	Modified images C10-CFA & C30-PATA mezzanine modules, added images C24-GBE (3rd Ethernet front panel jack option)	jj	24 November 2008
9	Added Power requirements for type -6-	vl	2009-02-20
10	Corrected section 'Replacement of the Battery'	jj	8 September 2010

Related Documents

- For information about the CCA-LAMBADA refer to the CCA Technical Information Manual, available at http://www.ekf.com/c/ccpu/cca/cca_tie.pdf
- For information about the CCB-BOSSANOVA refer to the CCB Technical Information Manual, available at http://www.ekf.com/c/ccpu/ccb/ccb_tie.pdf
- For information regarding the CDT-RIO rear I/O transition module please read the CDT Technical Information Manual, available at http://www.ekf.com/c/ccpu/cd3/cdt_tie.pdf
- For ordering information refer to document CD3-JIVE Product Information, available at http://www.ekf.com/c/ccpu/cd3/cd3_pie.pdf

Theme	Document Title	Origin
CompactPCI	*CompactPCI* Specification, PICMG 2.0 R3.0, Oct. 1, 1999	www.picmg.org
PCI Express	PCI Express™ Base Specification Revision 1.0a, April 15, 2003	www.pcisig.com
Ethernet	IEEE Std 802.3, 2000 Edition	standards.ieee.org
USB	Universal Serial Bus Specification	www.usb.org
Serial ATA	Serial ATA Revision 2.5	www.serialata.org
CompactFlash	CF+ and CompactFlash Specification Revision 2.0	www.compactflash.org
PMC	Common Mezzanine Card Family P1386/2.4a & P1386.1/2.4	www.ieee.org

Nomenclature

Signal names used herein with an attached '#' designate active low lines.

Trade Marks

Some terms used herein are property of their respective owners, e.g.

- Intel, Pentium, Celeron, Pentium M, Core Duo: ® Intel
- ***CompactPCI***: ® PICMG
- PCI Express: ® PCI-SIG
- Windows 2000, Windows XP: ® Microsoft
- EKF, ekf system: ® EKF

EKF does not claim this list to be complete.

Legal Disclaimer - Liability Exclusion

This manual has been edited as carefully as possible. We apologize for any potential mistake. Information provided herein is designated exclusively to the proficient user (system integrator, engineer). EKF can accept no responsibility for any damage caused by the use of this manual.

CD3-JIVE Features

Feature Summary

Feature Summary CD3-JIVE	
Form Factor	Double size *CompactPCI* style Eurocard (160x233mm^2), front panel width 4HP (20.3mm)
Processor	Designed for Intel® Pentium® M Micro FC-BGA 479 processors (90nm Dothan), maximum junction temperature 100°C ▸ CD3-2: 1.0GHz ULV Celeron® M (Dothan 373), 400MHz FSB, 512KB L2 cache, 5W ▸ CD3-3: 1.4GHz LV Pentium® M (Dothan 738), 400MHz FSB, 2MB L2 cache, 10W ▸ CD3-6: 2.0GHz Pentium® M (Dothan 760), 533MHz FSB, 2MB L2 cache, 27W
Chipset	Intel® i915 chipset (Alviso) consisting of: ▸ 82915GM Graphics/Memory Controller Hub (GMCH) with Intel® Graphics Media Accelerator (GMA) 900 ▸ 82801FB I/O Controller Hub (ICH6) ▸ 82802 Compatible Firmware Hub (FWH)
Memory	Dual 200-pin SO-DIMM socket, DDR2 533 (PC2) SDRAM, 2 x 1GB maximum, dual channel symmetric mode supported
Video	2 x DVI single or dual screen video output, up to 2048x1536 mode support, graphics controller with dual independent display pipes for different display timing and data on both outputs in single display mode, or dual screen mode for higher resolutions and refresh rates ▸ The lower DVI-I connector is suitable for both digital (DVI) and analog (VGA) displays, for attachment of VGA style monitors adapters and adapter cables are available ▸ The upper DVI-D connector is suitable for displays with DVI input only ▸ Front panel option: D-Sub (female HD15) VGA connector available, replaces DVI-I connector ▸ Rear I/O option: Analog video across J4/P4 suitable for CDT-RIO rear I/O transition module (VGA connector)
USB	All ports over-current protected, data transfer rate of up to 480Mbps, conforming to USB2.0: ▸ 2 x USB front panel connectors ▸ 4 x USB rear I/O ports across J4/P4 ▸ Suitable CDT-RIO rear I/O transition module provides 3 x USB back panel connectors + 1 x USB on-board connector ▸ 2 x USB ports available with proprietary expansion interface option (CCA-LAMBADA/CCB-BOSSANOVA mezzanine companion board)
Ethernet	▸ Triple 10/100/1000Mbps Gigabit Ethernet (GbE) controller ▸ One GbE Port software switchable (BIOS) between front panel and rear I/O ▸ Up to 2 x GbE accessible via RJ45 jacks from the front panel ▸ 3 x GbE via front panel (option) by means of special mezzanine PCB C24-GBE (replaces 2nd DVI) ▸ Up to 2 x GbE rear I/O according to PICMG® 2.16 across J3 ▸ Up to 2 x GbE rear I/O alternatively accessible via RJ45 jacks from the CDT-RIO back panel ▸ Jumbo Frame support up to 9KB
Serial Port (COM)	Available as an option, D-Sub 9-pin replaces DVI-D connector, RS-232E or RS-485 selectable
Mezzanine Facility PMC Module or SATA Storage Module	Optional usage of both: ▸ 1 Slot for a PMC module, I/O from the front panel and rear I/O across J5, dedicated PCIe to PCI bridge ▸ On-board Serial ATA dual 2.5-inch hard disk module C14-SATA, mounts on top of the PMC module space

Feature Summary CD3-JIVE

Proprietary Expansion Interface	▸ On-board LPC/USB/AC97 Super-I/O, USB and audio expansion interface connector ▸ Suitable CCA-LAMBADA 3U companion board available
Parallel ATA (IDE)	Single channel IDE I/F (2 devices): ▸ Ultra ATA/100 connector, handover to CCA-LAMBADA/CCB-BOSSANOVA mezzanine expansion board with optional on-board 2.5-inch IDE hard disk drive or external device ▸ CompactFlash socket for a CFA ATA memory card or Microdrive® (C10-1-CFA) ▸ Option 1.8-inch on-board hard disk module, replaces CompactFlash facility (C10-2-CFA)
Serial ATA	Quad-channel Serial ATA I/F: ▸ On-board SATA mezzanine storage module option (C14-SATA), 1 or 2 hard disk drives 2.5-inch, mass storage module mounts on top of the PMC slot space ▸ Up to 4 x SATA channels available for J3/P3 rear I/O option: SATA 0/1 can be routed either to the J3 or J5 rear I/O connector by means of a software controlled signal switch, and SATA 2/3 channels can be switched between J3 for rear I/O or P-SATA for on-board usage together with the C14-SATA mezzanine module ▸ Suitable rear I/O transition module CDT-RIO provides 3 x on-board SATA connectors and optionally 1 x eSATA connector (back panel External SATA)
CompactPCI	ICH6 integrated 32-bit PCI bridge, 133MBps CPCI master
Hot Swap Funktion	Board hot insertion/extraction without adversely effecting a running system, 'Basic Hot Swap' implementation according to CompactPCI Hot Swap Specification PICMG® 2.1. In order to use the CD3-JIVE as a peripheral slot board, special board versions are required (available on request).
Rear I/O J3/P3..J5/P5	▸ 4 x Serial ATA (2 x if on-board SATA storage module option is selected) ▸ 2 x GB Ethernet (1 port shared with front panel connector, selectable by BIOS) ▸ 4 x USB ▸ VGA Analog Video ▸ PS/2 Keyboard, Mouse ▸ COM1 (TTL Level), not available together with front panel connector option RS-232/RS-485 ▸ GPIO (TTL Level) ▸ AC '97 Audio ▸ Suitable rear I/O transition module CDT-RIO available
BIOS	▸ Phoenix BIOS with EKF embedded systems enhancements ▸ 8Mbit Flash memory ▸ Updates available from website ekf.com
Drivers (All Major OS)	▸ Intel graphics drivers ▸ Intel networking drivers

Typical Power Requirements

Board	+3.3V +0.17V/-0.1V		+5V +0.25V/-0.15V	
	MaxPower	WinXP Idle	MaxPower	WinXP Idle
CD3-2-JIVE	tbd	tbd	tbd	tbd
CD3-3-JIVE	tbd	tbd	tbd	tbd
CD3-6-JIVE	2,7A	2,3A	5,5A	1,6A

Thermal Conditions Environmental Conditions	▸ Operating temperature: 0°C ... +70°C (CPU dependent) ▸ Storage temperature: -40°C ... +85°C, max. gradient 5°C/min ▸ Humidity 5% ... 95% RH non condensing ▸ Altitude -300m ... +3000m ▸ Shock 15g 0.33ms, 6g 6ms ▸ Vibration 1g 5-2000Hz
EC Regulations	▸ EN55022, EN55024, EN60950-1 (UL60950-1/IEC60950-1) ▸ 2002/95/EC (RoHS)

Feature Summary CD3-JIVE			
MTBF	tbd		
Performance Rating Measured with PCMark2002 under Windows XP, 1GB DDR2 533	Board	Processor	CPU/MEM Score
	CD3-2-JIVE	1.0GHz ULV Celeron® M (Dothan 373)	tbd
	CD3-3-JIVE	1.4GHz LV Pentium® M (Dothan 738)	tbd
	CD3-6-JIVE	2.0GHz Pentium® M (Dothan 760)	tbd

Subject to technical changes

Short Description CD3-JIVE

Scalable from the ULV Celeron® M processor up to the 2.0GHz Pentium® M, and provided with 2GB dual channel capable DDR2 RAM, the CD3-JIVE is a versatile 6U/4HP (double size Eurocard) ***CompactPCI*** *® CPU board, designed especially for systems which require high performance at low power consumption.*

The Intel chipset is based on PCI Express technology and has a powerful integrated graphics accelerator. The CD3-JIVE is provided with two independent front panel DVI video connectors for simultaneous attachment of two flat panel displays.

If both video ports are active in single-channel mode, they can have different display timing and data. Alternatively the DVI ports can be combined for a dual screen configuration, supporting higher resolutions and refresh rates.

The CD3-JIVE is equipped with three independent Gigabit Ethernet controllers (including PICMG 2.16 support), and eight USB 2.0 ports for high speed communication.

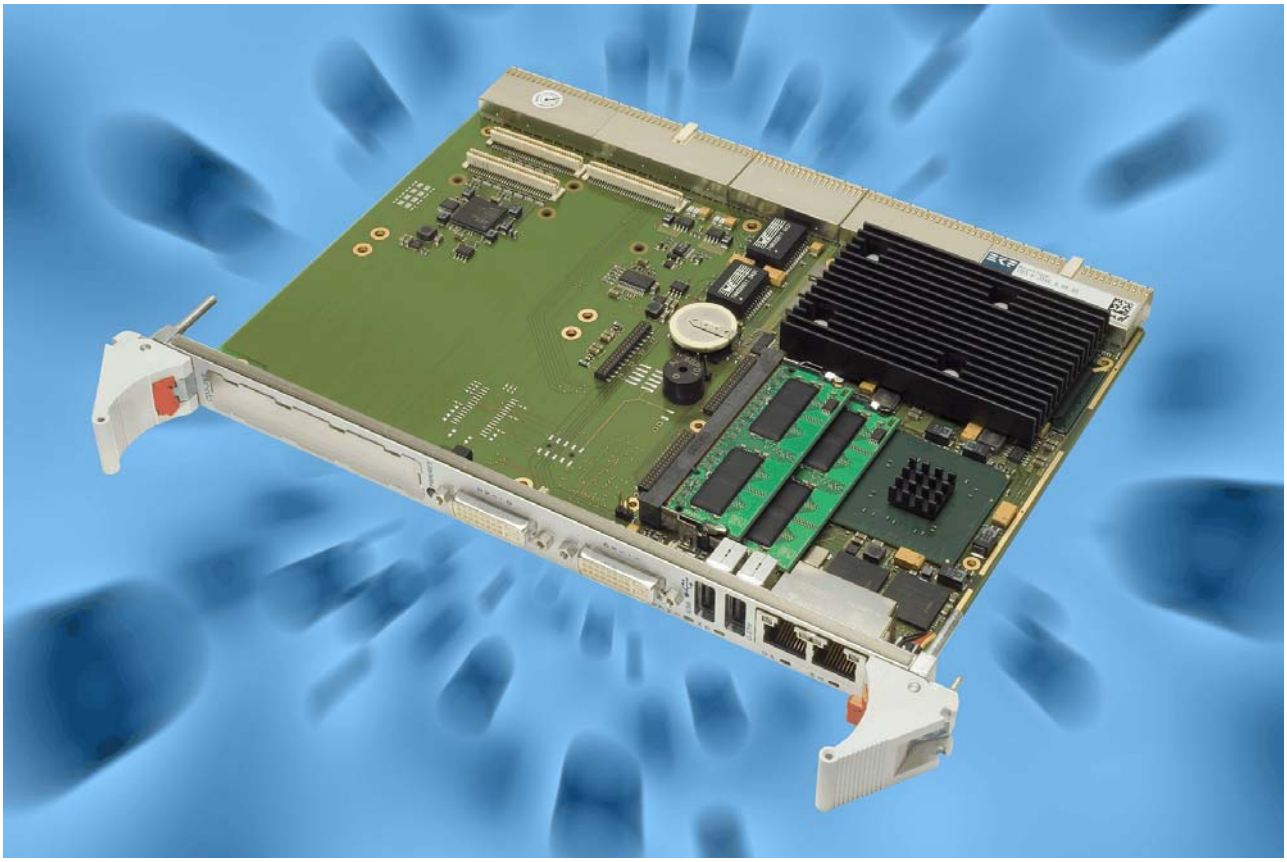
An on-board socket accommodates either a CompactFlash ATA card, or an 1.8-inch hard disk module.

A PMC mezzanine module connector may be used for individual system expansion. As an option, the CD3-JIVE is available in addition with a dual 2.5-inch SATA hard disk add-on module, which mounts on top of the PMC slot.

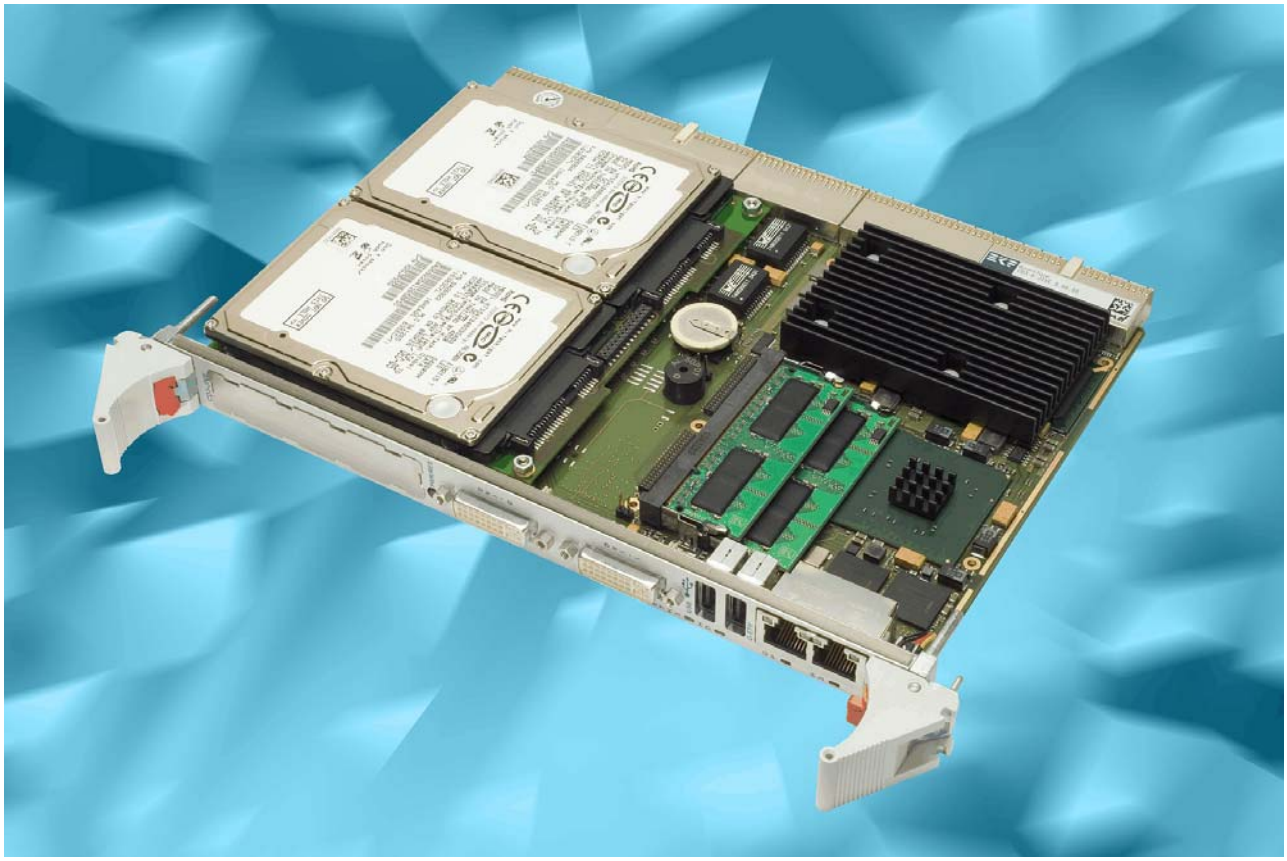
Furthermore, a rear I/O transition module is available for the CD3-JIVE. Four Serial ATA channels are routed across the J3-J5 CPCI connectors, besides two Gigabit Ethernet ports, four USB channels and a variety of other useful signals.

Benefits of the CD3-JIVE

- Pentium® M 2GHz (FSB 533MHz) CompactPCI CPU 6U/4HP
- PCI Express Chipset
- 2 x 1GB DDR2 Memory (Dual Channel Mode Capable)
- Dual-Screen Graphics Controller
- 3 x Gigabit Ethernet Controllers
- 4 x SATA I/F
- 8 x USB 2.0 Channels
- PMC Mezzanine Module Slot
- On-Board CompactFlash Card or 1.8-Inch Hard Disk Mezzanine Module
- Option on-Board Dual 2.5-Inch SATA Hard Disk Mezzanine Module
- Mezzanine Expansion Board and Rear I/O Transition Module Options
- RoHS compliant



CD3-JIVE Bare Bone View w/o Mezzanine Modules



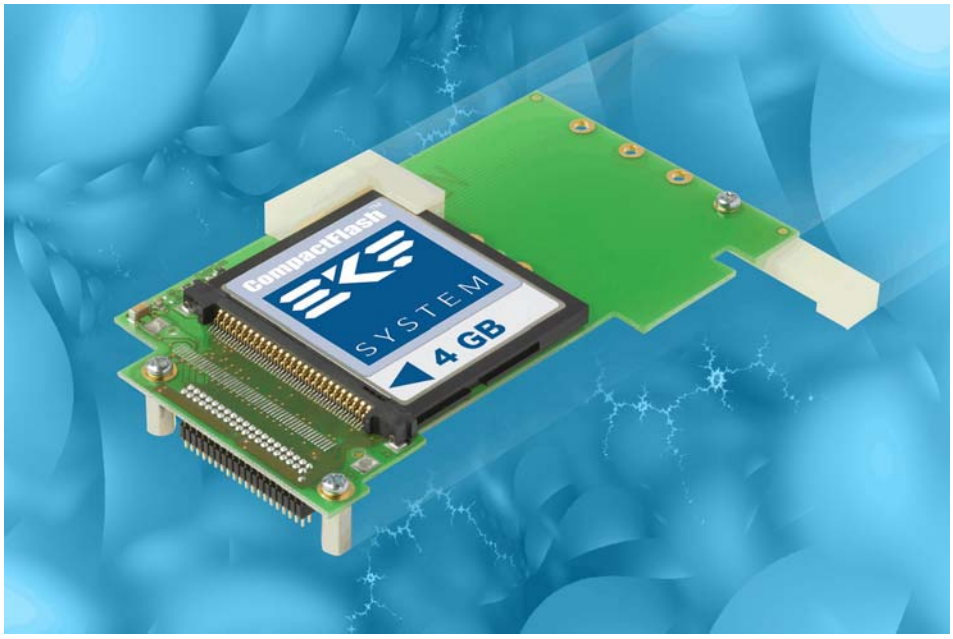
CD3-JIVE with C14-SATA

CD3-JIVE with on-Board CompactFlasch Module & DB1-FALCON PMC Module

CD3-JIVE with PMC Mezzanine Module DB1-FALCON & 1.8-Inch Hard Disk Drive

CD3-JIVE w. PMC Module & C14-SATA, 4HP Front Panel

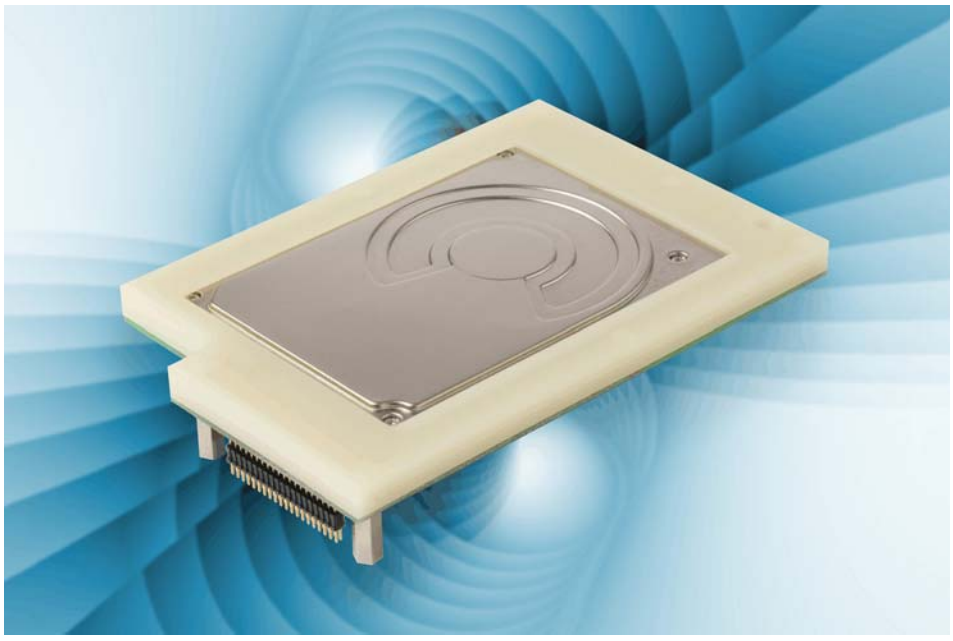
CD3-JIVE w. PMC Module & C14-SATA, 8HP Front Panel



CompactFlash Adapter Module for CD3-JIVE

The CD3-JIVE comes with a CompactFlash adapter module, which is suitable to hold a silicon memory CF card or Microdrive hard disk. If the CD3-JIVE is accompanied by a mezzanine expansion module such as the CCA-LAMBADA or CCB-BOSSANOVA, the position of the CompactFlash adapter module changes to the mezzanine card.

Optionally an on-board 1.8-inch hard disk module is available. When ordered, it replaces the CompactFlash adapter module (please request for a special solution which allows to use both the CF slot and the 1.8-inch drive simultaneously).

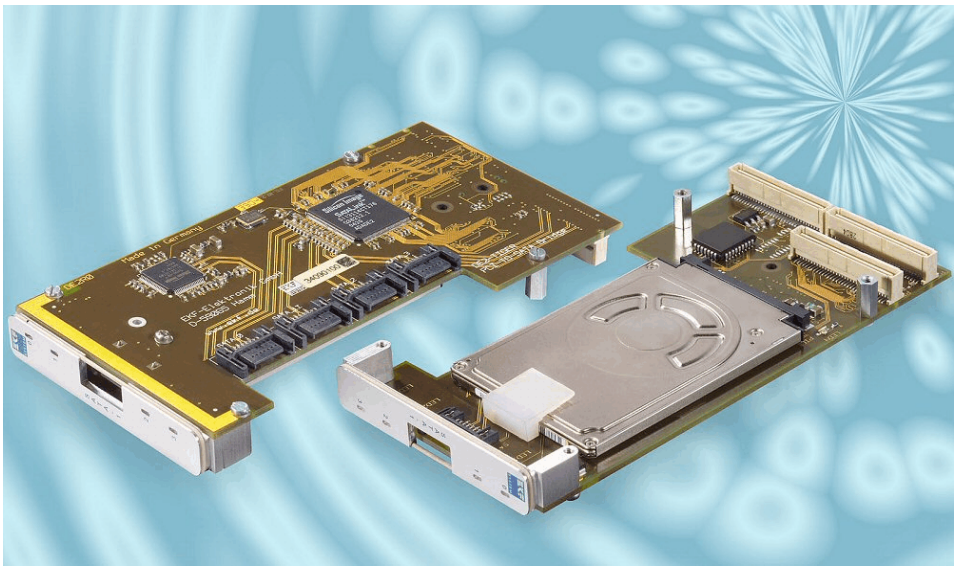


1.8-Inch on-Board Hard Disk Module for CD3-JIVE

C14-SATA Dual Serial ATA Hard Disk Mezzanine Module

In addition, the CD3-JIVE can be optionally ordered with a 2.5-inch SATA hard disk mezzanine module (C14-SATA, single or dual drive). This storage module option would normally occupy the mounting space which was originally reserved for the PMC module (4HP solution), but the PMC mezzanine module can also be placed underneath the C14-SATA module (8HP solution), and therefore the storage solution C14-SATA can be used in parallel with one PMC Module.

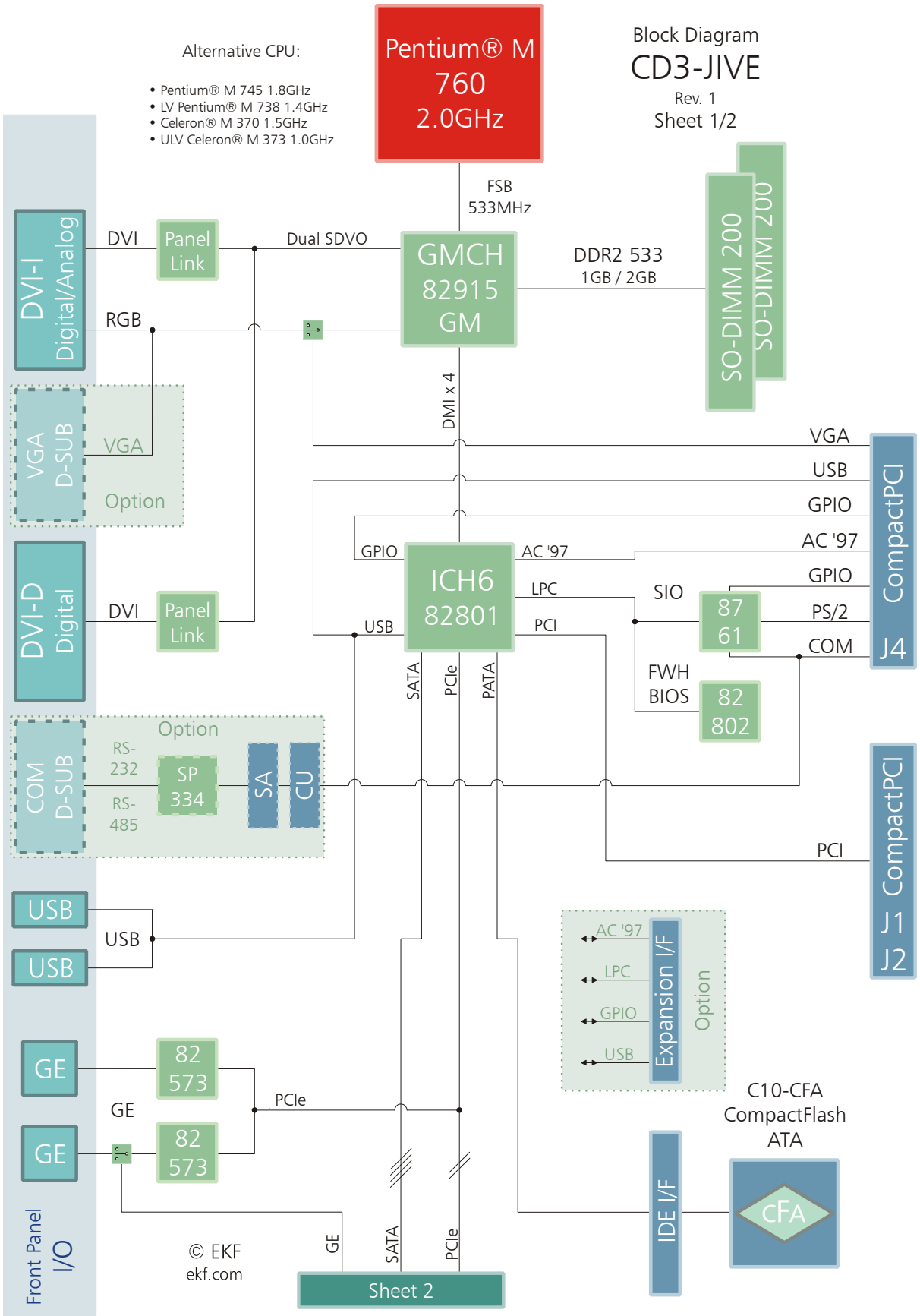
If the CD3-JIVE is equipped with the C14-SATA storage module, the number of SATA channels for rear I/O usage is limited to 2. The 2.5-inch hard disk module is an economical solution because its using the CD3-JIVE on-board SATA controller. There are several PMC based solutions available - the DE2-TIGER, a SATA/IDE controller PMC card with an integrated 1.8-inch drive. - DB1-FALCON, a Five Port USB 2.0 host controller, - for more available solutions please contact EKF..

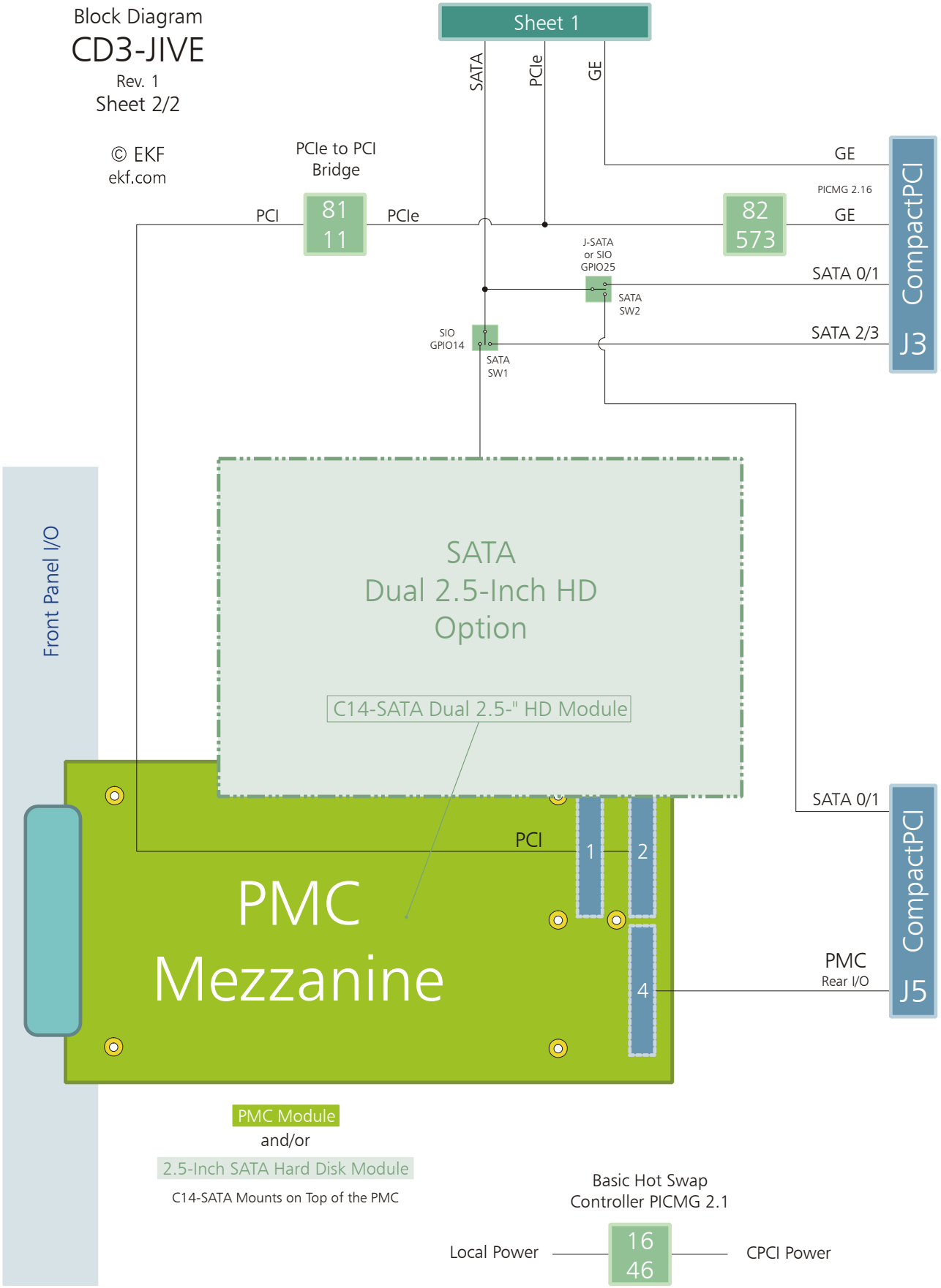


DE2-TIGER PMC Module with on-Board 1.8-Inch Hard Disk

CD3-JIVE 8HP Solution w. PMC Module, C14-SATA, CCA-LAMBADA

Block Diagram CD3-JIVE




Block Diagram
CD3-JIVE
Rev. 1
Sheet 2/2
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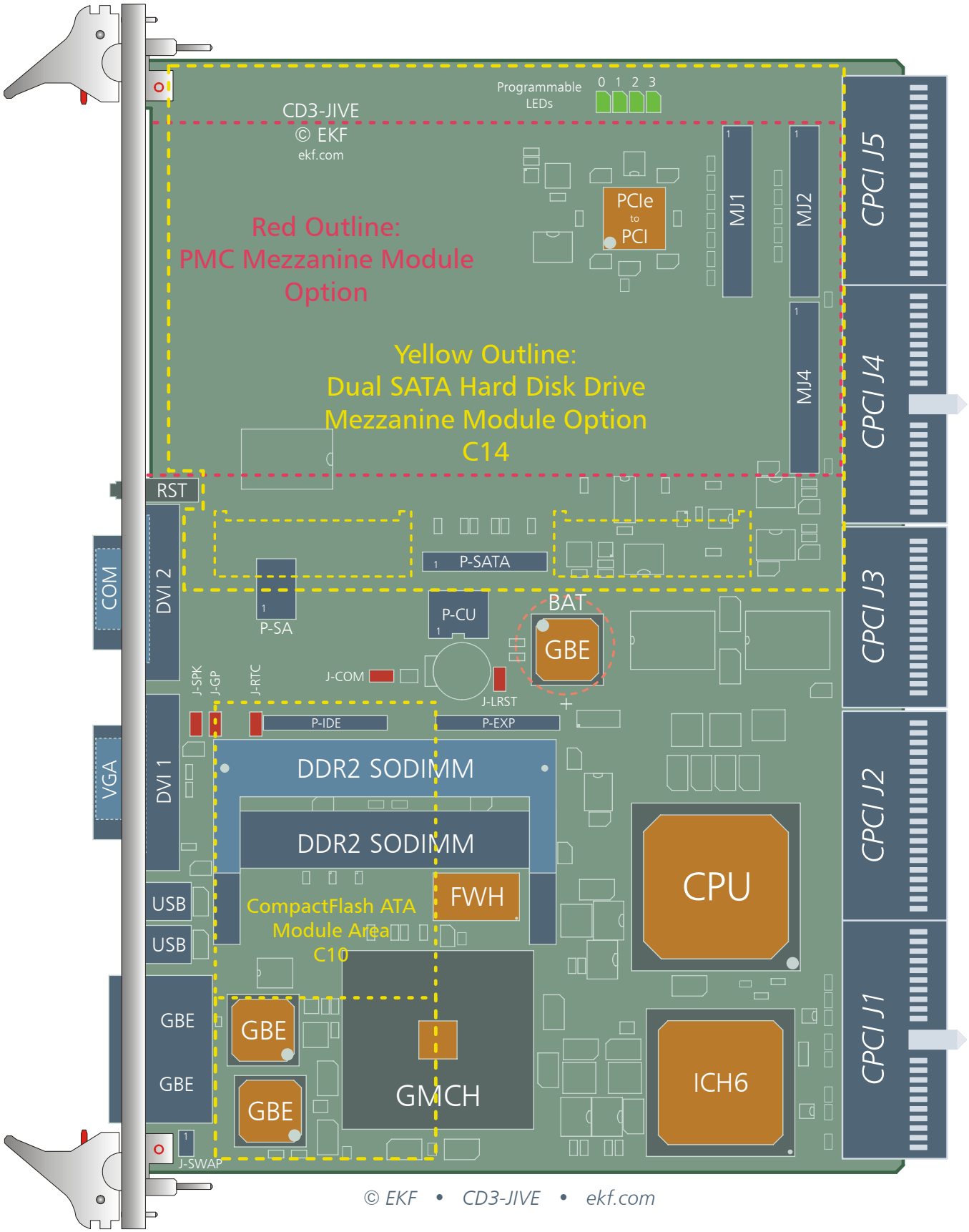
Sheet 1
SATA
PCIe
GE
PCIe to PCI Bridge
PCI
81 11
PCIe
82 573
GE
PICMG 2.16
CompactPCI J3
J-SATA or SIO GPIO25
SATA SW2
SATA 0/1
SIO GPIO14
SATA SW1
SATA 2/3
Front Panel I/O
SATA Dual 2.5-Inch HD Option
C14-SATA Dual 2.5-" HD Module
SATA 0/1
PCI
1
2
PMC Mezzanine
4
PMC Rear I/O
CompactPCI J5
PMC Module
and/or
2.5-Inch SATA Hard Disk Module
C14-SATA Mounts on Top of the PMC
Basic Hot Swap Controller PICMG 2.1
Local Power
16 46
CPCI Power

Top View Component Assembly CD3-JIVE



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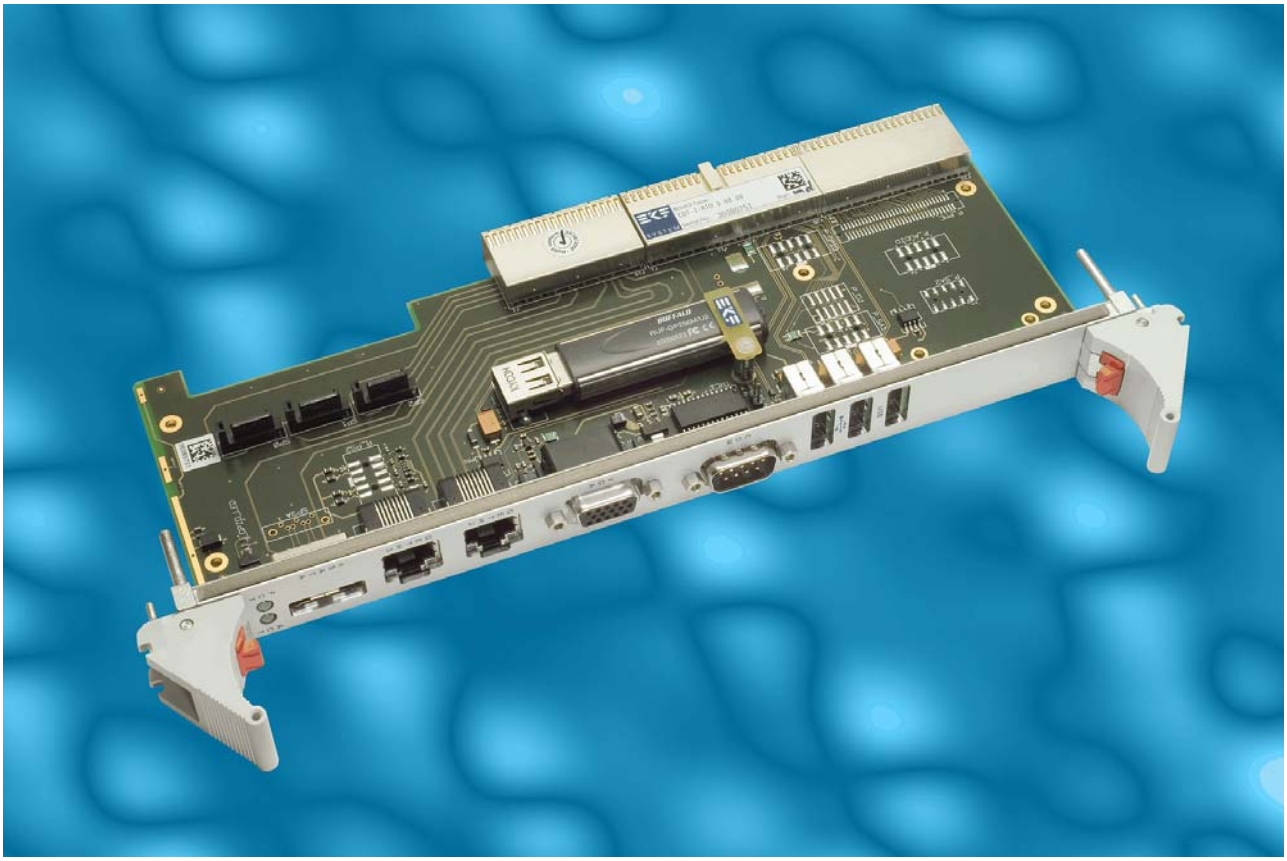
CDT-RIO Rear I/O Transition Module

Short Description

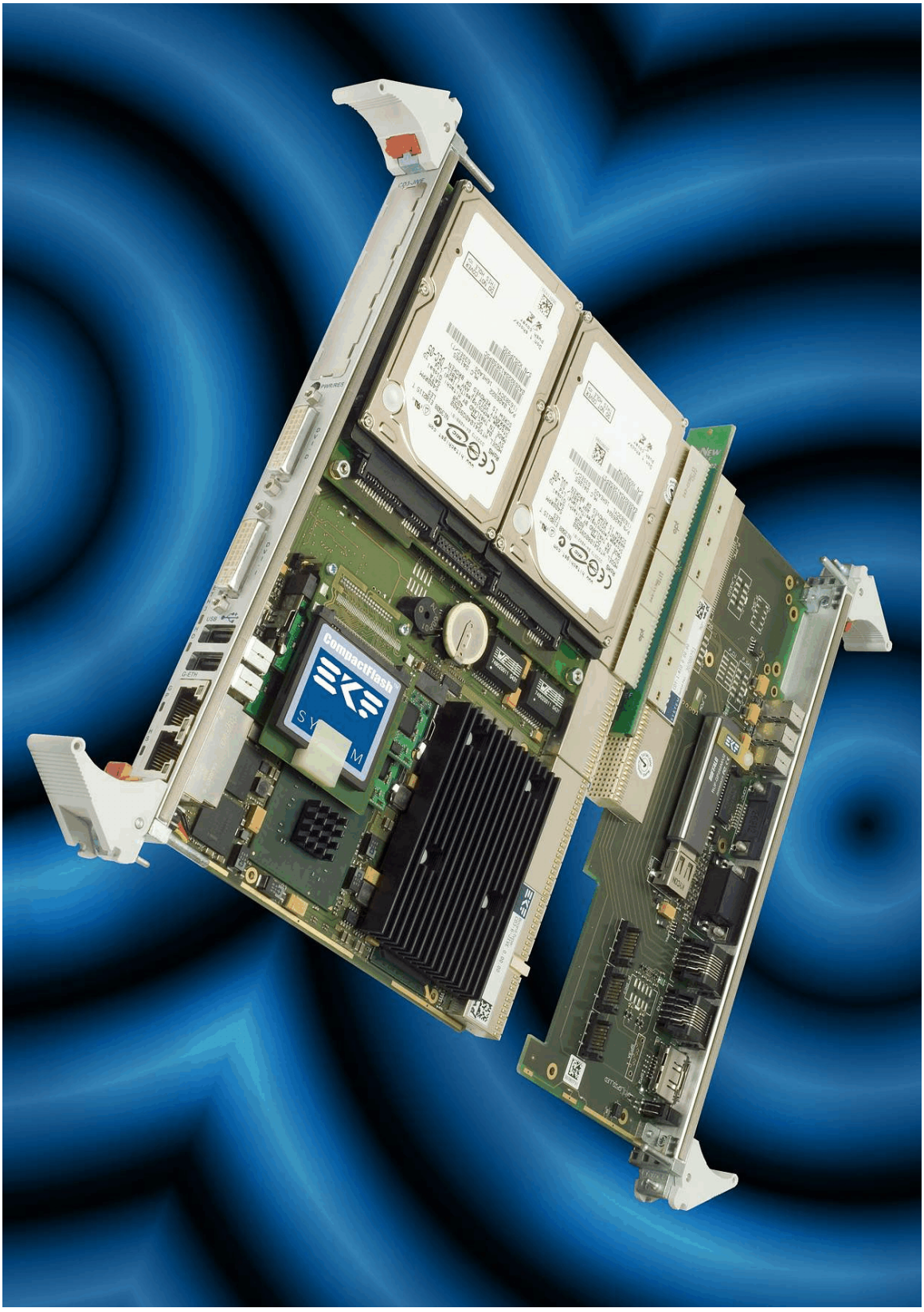
Available as a rear I/O expansion board to the CD3-JIVE CPU card, the CDT-RIO is provided with several I/O port connectors, to be used either in addition to the CD3-JIVE front panel connectors or alternatively. Being mainly a passive rear I/O transition module, groups of signals from the CD3-JIVE CPU board are passed across the CompactPCI J3-5/P3-5 connector to the CDT-RIO. Some of the data lines are available locally on the CDT board for system internal wiring only, while other connectors such as VGA-Video and Gigabit Ethernet are mounted into the back panel for external use. USB and SATA (eSATA) channels are provided both on-board and externally.

Typically the CDT-RIO is equipped with a 4-HP rear panel (20.3mm width). As a custom specific option, an 8-HP panel is available with additional connectors. Utilization of the CDT-RIO transition module adds a level of I/O functionality that is not available with the CD3-JIVE CPU board alone. Further on, swapping the CPU card is simplified by means of rear I/O, which is important for efficient system maintenance (MTTR).

For technical details please refer to the 'CDT-RIO Technical Information Manual', available at www.ekf.com/c/ccpu/cd3/cdt_tie.pdf.

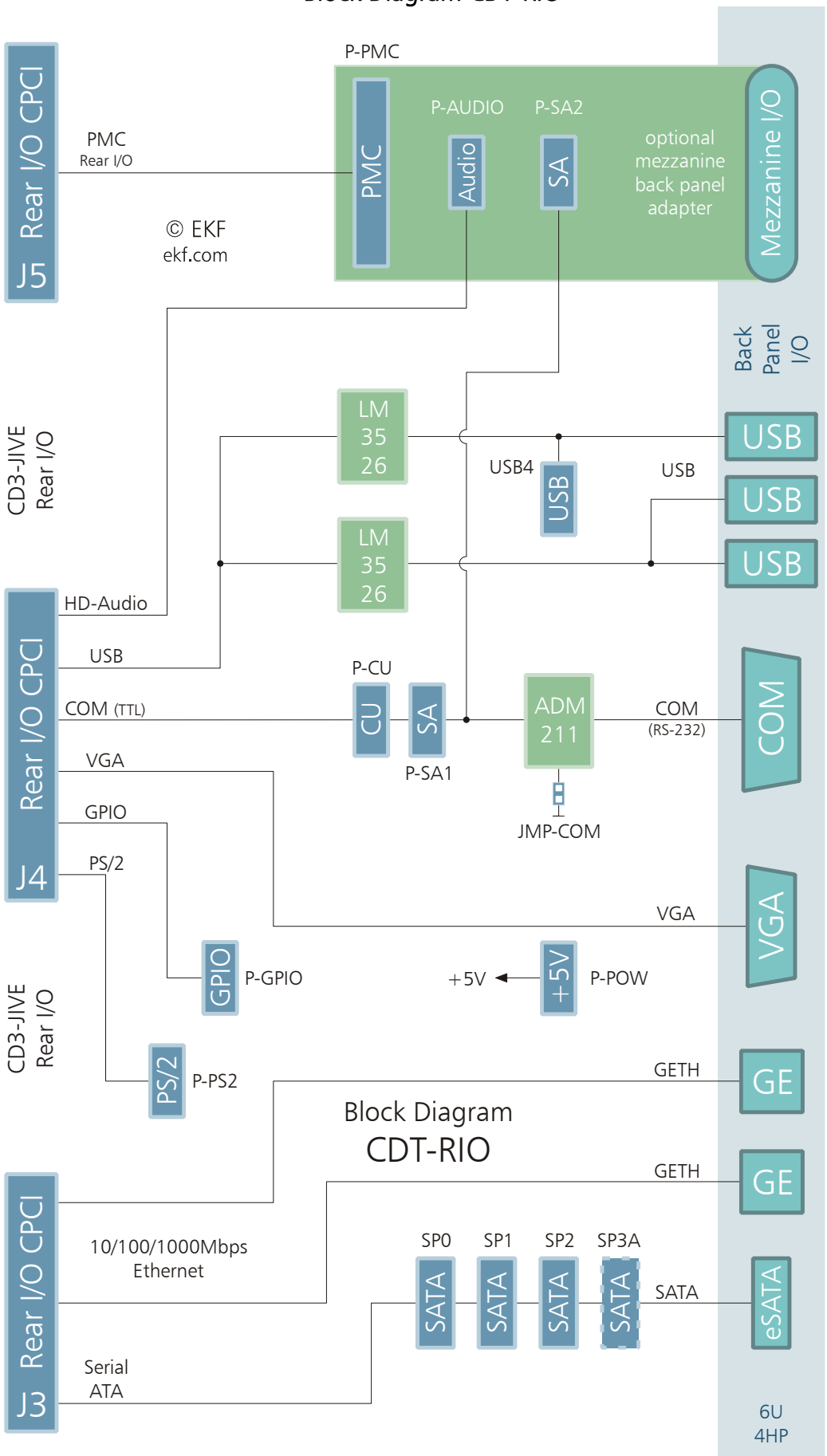


CDT-RIO Rear I/O Transition Module (Option)

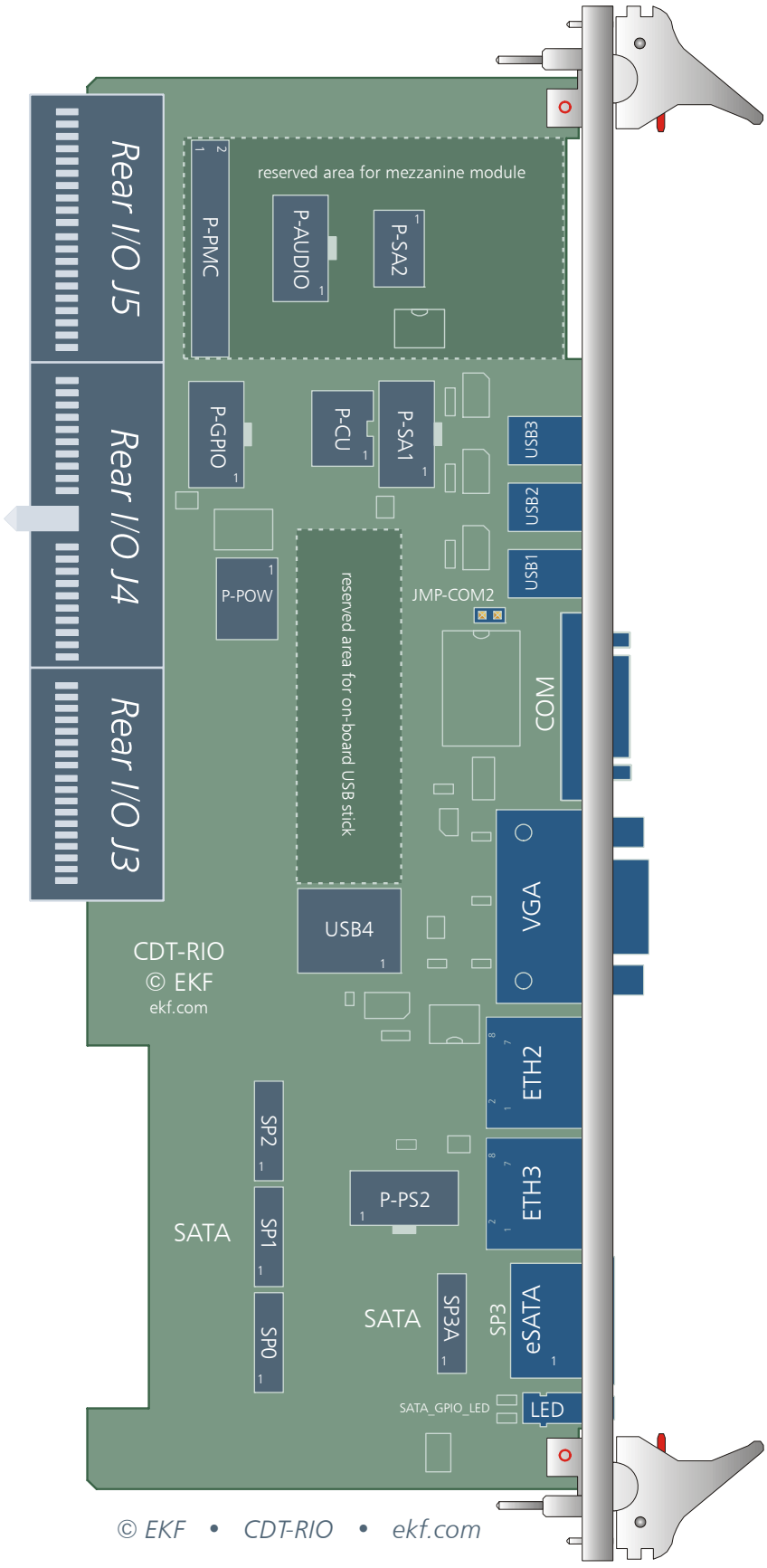


CD3-JIVE with CDT-RIO

Block Diagram CDT-RIO



Assembly Drawing CDT-RIO



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CD3-JIVE On-Board Elements

Strapping Headers

ISPCON	PLD programming connector, not stuffed
J-GP	Jumper to reset BIOS CMOS RAM values
J-LRST	Jumper to reset Board
J-RTC	Jumper to reset RTC core of ICH6, not stuffed
J-SPK	Speaker connector
JSWAP	Hot Swap Micro Switch Connector
JSATA	SATA switch CPCI J3/J5, not stuffed

Connectors & Sockets

J1/J2	*CompactPCI* Bus 32-bit, 33MHz, PXI Trigger
J3/J4/J5	*CompactPCI* Rear I/O
MJ1/2/4	PMC mezzanine module connectors, 32-bit PCI, rear I/O option
P-CU	UART COM port (TTL level) pin header provided for an optional EKF CU-series PHY module
P-EXPT P-EXPB	Expansion interface connector for optional mezzanine companion boards such as CCA-LAMBADA or CCB-BOSSANOVA, available either from top (T) or bottom (B) of the CD3-JIVE board
P-IDET P-IDEB	Ultra ATA/100 IDE port, either for C10-CFA mezzanine module with CompactFlash Card or 1.8-Inch ATA hard disk, or optional mezzanine companion boards such as CCA-LAMBADA or CCB-BOSSANOVA, available either from top (T) or bottom (B) of the CD3-JIVE board
P-ITP	CPU debug port
P-SA	UART COM port (TTL level) connector provided for an optional MEN SA-type PHY mezzanine module
P-SATA	Serial ATA mezzanine module connector, provided for the C14-SATA dual hard disk option
SODIMM1 SODIMM2	200-pin DDR2 memory module SDRAM PC2-3200/4200 (DDR400/533) sockets

LED Indicators

LED0 ... 3	User programmable LEDs (option)

CD3-JIVE Front Panel Elements

GBE 1 GBE 2	1000Base-TX/100Base-TX/10Base-T, RJ-45 receptacles with integrated indicator LEDs activity & speed
USB1/2	Universal Serial Bus 2.0 self powered root hub, type A receptacle
DVI 1 VGA	DVI-I integrated (digital & analog) receptacle, suitable for DVI digital flat panel displays and/or analog monitors Option VGA D-Sub connector
DVI 2 COM	DVI-D (digital-only) receptacle, suitable for DVI digital flat panel displays Option CU/SA-type mezzanine module or COM port connector
PMC	PMC mezzanine module front panel connector(s)
GP	General Purpose LED
HD	LED indicating any activity on IDE or SATA ports
HS	Hot swap LED (Blue)
ETH3	Activity LED rear panel (or PICMG 2.16 backplane) GBE port
Reset (PWR/RES)	Reset push-button switch with integrated indicator LED (power good)

Microprocessor

The CD3-JIVE is designed for use with Pentium® M and Celeron® M processors manufactured in 90nm technology (Dothan). These include also the Ultra Low-Voltage (ULV) Celeron® M and the Low-Voltage (LV) Pentium® M processors as listed below. The processors are housed in a Micro FC-BGA package for direct soldering to the PCB, i.e. the CPU chip cannot be removed or changed by the user.

The processors supported by the CD3-JIVE are running at FSB clock speeds of 400MHz and 533MHz. The internal Pentium M processor speed is achieved by multiplying the host bus frequency by a variable value. The multiplier is chosen by currently required performance and the actual core temperature. This technology is called Enhanced Intel SpeedStep®.

Power is applied across the *CompactPCI* connectors J1 (3.3V, 5V). The processor core voltage is generated by a switched voltage regulator, sourced from the 5V plane. The processor signals its required core voltage by 6 dedicated pins according to Intels IMVP-IV voltage regulator specification.

90nm (Dothan) Processors Supported								
Processor	Speed min/max [GHz]	Host Bus [MHz]	L2 Cache [MB]	TDP [W]	Die Temp [°C]	CPU ID	Stepping	sSpec
ULV Celeron M 373 [1) 2)]	1.0/1.0	400	0.5	5	0-100	06D8h	C-0	SL8LW
LV Pentium M 738 [2)]	0.6/1.4	400	2	10	0-100	06D6h 06D8h	B-1 C-0	SL7P9 SL89N
Pentium M 745 [2)]	0.6/1.8	400	2	21	0-100	06D6h 06D8h	B-0 C-0	SL7Q6 SL8U8
Pentium M 760 [2)]	0.8/2.0	533	2	27	0-100	06D8h	C-0	SL869

1) This processor does not support SpeedStep® technology, thus it runs at a fixed core speed.
2) Following the Intel Embedded Roadmap, this processor is recommended for long time availability.

Thermal Considerations

In order to avoid malfunctioning of the CD3-JIVE, take care of appropriate cooling of the processor and system, e.g. by a cooling fan suitable to the maximum power consumption of the CPU chip actually in use. Please note, that the processors temperature is steadily measured by a special controller (LM87), attached to the onboard SMBus® (System Management Bus). A second temperature sensor internal to the LM87 allows for acquisition of the boards surface temperature. Beside this the LM87 also monitors most of the supply voltages. A suitable software to display both, the temperatures as well as the supply voltages, is MBM (Motherboard Monitor), which can be downloaded from the web. After installation, both temperatures and voltages can be observed permanently from the Windows taskbar.

The CD3-JIVE is equipped with a passive heatsink. Its height takes into account the 4HP limitation in mounting space of a CPCI board. In addition, a forced vertical airflow through the system enclosure (e.g. bottom mount fan unit) is strongly recommended (>15m^3/h or 200LFM around the CPU slot). As an exception, the CD3-2-JIVE (ULV Celeron M 1GHz) can be operated with natural convection only. Be sure to thoroughly discuss your actual cooling needs with EKF. Generally, the faster the CPU speed the higher its power consumption. For higher ambient temperatures, consider increasing the forced airflow to 400 or 600LFM.

The table showing the supported processors above give also the maximum power consumption (TDP = Thermal Design Power) of a particular processor. Fortunately, the power consumption is by far lower when executing typical Windows or Linux tasks. The heat dissipation increases when e.g. rendering software like the Acrobat Distiller is executed.

The Pentium M processors support Intel's Enhanced SpeedStep® technology. This enables dynamic switching between multiple core voltages and frequencies depending on core temperature and currently required performance. The processors are able to reduce their core speed and core voltage in up to 8 steps down to 600MHz. This leads to an obvious reduction of power consumption (max. 7.5W @600MHz) resulting in less heating. This mode of lowering the processor core temperature is called TM2 (TM=Thermal Monitor). Note, that TM2 is not supported by Celeron M processors.

Another way to reduce power consumption is to modulate the processor clock. This mode (TM1) is supported also by the Celeron M processors and is achieved by actuating the 'Stop Clock' input of the CPU. A throttling of 50% e.g. means a duty cycle of 50% on the stop clock input. However, while saving considerable power consumption, the data throughput of the processor is also reduced. The processor works at full speed until the core temperature reaches a critical value. Then the processor is throttled by 50%. As soon as the high temperature situation disappears the throttling will be disabled and the processors runs at full speed again.

A similar feature is embedded within the Graphics and Memory Controller (GMCH) i915GM. An on-die temperature sensor is used to protect the GMCH from exceeding its maximum junction temperature ($T_{J,max}$=105°C) by reducing the memory bandwidth.

These features are controllable by BIOS menu entries. By default the BIOS of the CD3-JIVE enables mode TM2 which is the most efficient.

Main Memory

The CD3-JIVE is equipped with two sockets for installing 200-pin SO-DIMM modules (module height = 1.25 inch). Supported are unbuffered DDR2 SO-DIMMs (V_{CC}=1.8V) without ECC featuring on-die

termination (ODT), according the PC2-3200 or PC2-4200 specification. Minimum memory size is 128MB; maximum memory size is 2GB. Due to the video requirements of the i915GM chipset, a minimum of 2x256MB of memory is recommended for the operating systems Windows NT 4.0, Windows 2000 or Windows XP (some of the system memory is dedicated to the graphics controller). The contents of the SPD EEPROM on the SO-DIMMs is used by the BIOS at POST (Power-on Self Test) to program the memory controller within the chipset.

The i915GM chipset supports symmetric and asymmetric memory organization. The maximum memory performance can be obtained by using the symmetric mode. To achieve this mode two SO-DIMMs of equal capacity must be installed in the memory sockets. In asymmetric mode different memory modules may be used with the drawback of less bandwidth. A special case of asymmetric mode is to populate only one memory module (i.e. one socket may be left empty).

LAN Subsystem

The Ethernet LAN subsystem is composed of three Intel 82573 Gigabit Ethernet controllers that provide also legacy 10Base-T and 100Base-TX connectivity. Two Ethernet ports are fed to two RJ45 jacks located in the front panel (one is configurable as an alternative to backplane packet switching according PICMG Spec 2.16, or CDT-RIO rear panel I/O). The third Ethernet controller is solely available for backplane packet switching or rear panel I/O. Each port includes the following features:

- One PCI Express lane per Ethernet controller (250MB/s)
- 1000Base-Tx (Gigabit Ethernet), 100Base-TX (Fast Ethernet) and 10Base-T capability
- Half- or full-duplex operation
- IEEE 802.3 Auto-Negotiation for the fastest available connection
- Jumperless configuration (complete software-configurable)
- Two bicoloured LEDs integrated into the dedicated RJ-45 connectors to signal the LAN link, the LAN connection speed, and activity status.

Each NIC (Networking Interface Controller) is connected by a single PCI Express lane to the chipset (ICH6). Their MAC addresses (unique hardware numbers) are stored in dedicated EEPROMs. The Intel Ethernet software and drivers for the 82573 is available from Intel's website for download.

Serial ATA Interface (SATA)

The CD3-JIVE provides four serial ATA (SATA) ports, each capable of transferring 150MB/s. Integrated within the ICH6, the SATA controller features different modes to support also legacy operating systems.. The four SATA channels are routed to the CompactPCI J3 connector, thus they are accessible via the rear I/O transition module CDT-RIO.

Two serial ATA ports could be switched alternately to an onboard connector suitable for mounting C14-SATA. The other two SATA channels could be switched between CompactPCI J3 an CompactPCI J5

A LED named HD located in the front panel, signals disk activity status of the SATA and IDE devices.

Available for download from Intel's web site are drivers for popular operating systems, e.g. Windows® 2000, Windows® XP and Linux.

Enhanced IDE Interface

The EIDE interface handles the exchange of information between the processor and legacy mass storage peripheral devices like hard disks, ATA CompactFlash cards and CD-ROM drives. The interface supports:

- Up to two parallel ATA devices
- PIO Mode 3/4, Ultra ATA/33, Ultra ATA/66, Ultra ATA/100

The IDE interface is routed to the on-board connectors P-IDET and P-IDEB (T:top side, B:bottom side of the board). P-IDE is used to interface to the CompactFlash Card adapter C10-CFA or to the expansion board CCA-LAMBADA. Use the C10-CFA adapter to attach a CompactFlash ATA style silicon disk, whenever a hard disk is not suitable for your system, or as an additional mass storage device. The CCA-LAMBADA expansion board is capable to carry an on-board 1.8" or 2.5" hard disk drive. When using the 1.8" option the concurrent operation of a CompactFlash device is possible.

A LED named HD located in the front panel signals the disk activity status of both the IDE and SATA devices.

The IDE controller is integrated into the ICH6. Ultra ATA IDE drivers can be downloaded from the Intel web site.

Graphics Subsystem

The graphics subsystem is part of the Intel i915GM Graphics/Memory Controller Hub (GMCH) and supports dual screen operation. The CD3-JIVE therefore is provided with a DVI-I (DVI 1) and in addition a DVI-D (DVI 2) graphics connector. DVI-I is both a digital and analog interface, DVI-D is only a digital interface. Recent digital input flat-panel displays are widely available with this connector style. For classic monitors, adapters or adapter cables can be used for converting from DVI-I to the 15-pin HD D-SUB connector.

A special display transmitter chip is used to convert Intel's proprietary, PCI express based SDVO interface to the differential DVI signals. The SiI1362 (Silicon Image) transmitter uses PanelLink® Digital technology to support displays ranging from VGA to UXGA resolutions (25 - 165Mpps) in a single link interface.

The GMCH supports several video resolutions and refresh rates. A partial list is contained in the table below. Please note, that flat-panel displays should be operated with their maximum resolution at 60Hz refresh rate.

Partial List of i915GM GMCH Video Modes (analog / digital)					
Resolution	60Hz	70Hz	72Hz	75Hz	85Hz
640x480	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
800x600	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
1024x768	✓ / ✓[1)]	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
1280x1024	✓ / ✓[1)]	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
1600x1200	✓ / ✓[1)]	✓ / -	✓ / -	✓ / -	✓ / -
2048x1536	✓ / -	✓ / -	✓ / -	✓ / -	- / -

[1)] This video mode is suitable for popular flat-panel displays.

As an alternative option to the DVI 1 receptacle, the CD3-JIVE can be equipped with an ordinary HD D-Sub 15-lead connector (VGA style). This connector is suitable for analog signals only, so the PanelLink transmitter is not stuffed with this option. Nevertheless also flat-panel displays can be attached to the D-Sub connector but with minor reduced image quality.

Independent from the video connector actually in use, DVI or VGA, the VESA DDC 2B standard is supported. This is a two-wire serial bus (clock, data), which is controlled by the GMCH and allows to read out important parameters, e.g. the maximum allowable resolution, from the attached monitor. In addition, DDC Power (+5V) is delivered to either connector. A resettable fuse is stuffed to protect the board from an external short-circuit condition (0.75A).

Graphics drivers for the i915GM can be downloaded from the Intel web site.

Real-Time Clock

The CD3-JIVE has a time-of-day clock and 100-year calendar, integrated into the ICH6. A battery on the board keeps the clock current when the computer is turned off. The CD3 uses a BR2032 lithium battery soldered in the board, giving an autonomy of more than 3 years. Under normal conditions, replacement should be superfluous during lifetime of the board.

Universal Serial Bus (USB)

The CD3-JIVE is provided with eight USB ports, all of them are USB 2.0 capable. Two USB interfaces are routed to front panel connectors, two ports are feed to the expansion board interface connectors P-EXP, and four ports are optionally available for rear I/O across the J4/P4 *CompactPCI* connector.

The front panel USB connectors can source up to 0.5A/5V each, over-current protected by two electronic switches. Protection for the USB ports on the expansion interface and on the rear I/O connector is located on the CCA-LAMBADA and the CDT-RIO respective. The USB controllers are integrated into the ICH6.

LPC Super-I/O Interface

In a modern system, legacy ports as PS/2 keyboard/mouse, COM1/2 and LPT have been replaced by USB and Ethernet connectivity. The 1.4MB floppy disk drive has been swapped against CD-RW drives, attached to a SATA connector, or USB memory sticks. Hence, the CD3-JIVE is virtually provided with all necessary I/O ports. However, for compatibility purposes the CD3-JIVE is additionally equipped with a simple Super-I/O chip, for optional rear I/O of PS/2 keyboard/mouse and COM1 (TTL level only) across the J4/P4 CPCI connector. COM1 is also available as front panel connector option, if the DVI 2 video connector would not be needed (requires a SA-type PHY module attached to P-SA). The Super-I/O controller resides on the local LPC bus (LPC = Low Pin Count interface standard), which is a serialized ISA bus replacement.

As an alternative, EKF offers the CCA-LAMBADA or CCB-BOSSANOVA mezzanine expansion modules to the CD3-JIVE, featuring all classic Super-I/O functionality. The CCA-LAMBADA is a 3U Eurocard with a 4HP (single) width front panel. Access to the connectors PS/2 (mouse, keyboard), COM, USB and audio in/out is given directly from the front panel. The CCA-LAMBADA connects to the CD3-JIVE across the connector P-EXPT or P-EXPB, hence the CCA-LAMBADA can be attached either to the top or to the bottom of the CD3-JIVE.

Reset/Watchdog

The CD3-JIVE is provided with two supervisor circuits to monitor the supply voltages 1.8V, 3.3V, 5V, and to generate a clean power-on reset signal.

The reset manual push-button is situated at the front panel. The button is indent mounted behind the front and requires a tool, e.g. pen to be pressed, preventing from being inadvertently activated. The push button reset signal is routed across a PLD (programmable logic device) and could be inhibited on customers request.

An alternative way to generate a system reset is to activate the signal PRST# located on CompactPCI connector J2 pin C17. Pulling this signal to GND will have the same effect as to push the handle's red push button.

The healthy state of the CD3-JIVE is signalled by the LED PG (Power Good) located in the front panel. As soon as this LED begins to shine all power voltages are within their specifications and the reset signal has been deasserted.

An important reliability feature is the watchdog function, which is programmable by software. The behaviour of the watchdog is defined within the PLD, which activates/deactivates the watchdog and controls its time-out period. The time-out delay is adjustable in the steps 2, 10, 50 and 255 seconds. After alerting the WD and programming the time-out value, the related software (e.g. application program) must trigger the watchdog periodically. All watchdog related functions are made available by calling service requests within the BIOS.

The watchdog is in a passive state after a system reset. There is no need to trigger it at boot time. The watchdog is activated on the first trigger request. If the duration between two trigger requests exceeds the programmed period, the watchdog times out and a system reset will be generated. The watchdog remains in the active state until the next system reset. There is no way to disable it once it had been put on alert, whereas it is possible to reprogram its time-out value at any time.

Firmware Hub (Flash BIOS)

The BIOS is stored in an 82802 8Mbit Firmware Hub (there are second sources in use with deviant part numbers). The firmware hub contains a nonvolatile memory core based on flash technology, allowing the BIOS to be upgraded.

The FWH can be reprogrammed (if suitable) by a DOS based tool. This program and the latest CD3-JIVE BIOS are available from the EKF website. Read carefully the enclosed instructions. If the programming procedure fails e.g. caused by a power interruption, the CD3-JIVE may no more be operable. In this case you would have to send in the board, because the BIOS is directly soldered to the PCB and cannot be changed by the user.

Mezzanine Interfaces

The PMC mezzanine card socket enables on-board expansion of the CD3-JIVE.
The PMC slot on the CD3 supports a 32-bit/66MHz PCI interface with VI/O=3.3V. The modules rear I/O is wired to the CompactPCI connector J5. Alternatively I/O can be obtained via the front panel connector of the module (if any).

As an option, the CD3-JIVE is also available with a dual 2.5-inch SATA hard disk add-on module (C14-SATA), which occupies the PMC slot.

PG (Power Good) LED

The CD3-JIVE offers a software programmable LED located in the reset push-button. After system reset, this LED defaults to signal the board healthy respective power good state. This LED changes its function by calling an appropriate BIOS request and is then controlled by software only. The PG LED remains in the programmable state until the next system reset occurs.

HD (Hard Disk Activity) LED

The CD3-JIVE offers a LED, marked as HD (placed within the front panel). This LED signals activity on any device attached to the SATA or the IDE ports.

GP (General Purpose) LED

A second, programmable LED can be also observed from the front panel. The status of the GP LED is controlled by the GPO18 output of the ICH6. Setting this pin to 1 will switch on the LED. As of current, the GP LED is not dedicated to any particular hardware or firmware function (this may change in the future).

Hot Swap Detection

The CD3-JIVE uses a LTC1646 hot swap power controller. The main task of this device is a controlled switching of the board power supplies. On-board insertion the various power planes on the board (3.3V, 5V, ±12V) are ramped up slowly to avoid too large voltage drops within the system. When all voltages have reached their nominal values the controller asserts the CompactPCI signal HEALTHY# (connector J1 pin B4). Electronic circuit breakers protect +3.3V and +5V against overcurrent fault conditions. As soon as the current on these supplies exceed a value of 11A, the power of all supplies (including ±12V) are switched off and the fault is flagged to the system by deasserting the HEALTHY# signal.

The CompactPCI specification added the signal ENUM# to the PCI bus to allow the system hot swapping. This signal is routed to the GPI3 of the ICH6 on the CD3-JIVE. A System Management Interrupt (SMI) can be requested if ENUM# changes by insertion or removal of a board.

Blue Hot Swap LED
The CD3-JIVE is equipped with a blue LED (a LED marked as HS is placed in the front panel near the lower board handle), that indicates when board extraction is permitted. A micro switch in one of the front panel ejectors signals when a board extraction event takes place. This micro switch is connected via the 3-pin header JSWAP.

Power Supply Status (DEG#, FAL#)

Power supply failures may be detected before the system crashes down by monitoring the signals DEG# or FAL#. These active low lines are additions of the *CompactPCI* specification and may be driven by the power supply. DEG# signals the degrading of the supply voltages, FAL# there possible failure. On the CD3-JIVE the signal FAL# is routed to the GPI4 and DEG# to the GPI5 of the ICH6.

PXI Trigger Signals

As a stuffing option (resistor network), the CD3-JIVE supports four of the eight trigger signals of the PXI standard across the connector J2, as defined by National Instruments. The trigger signals are provided by the local SIO (Super-I/O) chip IT8761E. GPIO20/21 are routed to TRIG0/1, and GPIO26/27 are used to control TRIG6/7. These signals may alternatively be used as GPIO lines in a non-PXI environment.

GPIO Signals

As an alternative, the IT8761E GPIO20/21 and GPIO26/27 are also available from the rear I/O connector J4 (stuffing option by means of a resistor network). In addition, the IT8761E GPIO22 .. GPIO24 are permanently wired to J4. GPIO25 is (default) used for switching SATA signals between CompactPCI J3 and CompactPCI J5. As a stuffing option GPIO25 could be wired to J4.

In addition to the GPIO lines listed above available for rear I/O on J2 and/or J4, the expansion connector P-EXP provides another two GPIO lines available for user specific application. The 5V TTL signals sio_gpio16/17 are controlled by the on-board SIO IT8761E, with an internal 50kΩ PU resistor and capable of sinking 24mA each.

Rear I/O Options

Optionally, the CD3-JIVE can be used for rear I/O with respect to the following functions:

- 2 x Gigabit Ethernet - J3
- 4 x SATA (up to 4 x SATA, 1 x eSATA) - J3
- Analog video (VGA) - J4
- 4 x USB - J4
- PS/2 keyboard & mouse - J4
- COM1 (TTL level) - J4
- GPIO - J4
- PMC mezzanine module rear I/O - J5

The analog graphics and the Gigabit Ethernet port 1 lines are routed to signal multiplexers on the CD3-JIVE. These analog signal switches, controlled by the BIOS, select either the front panel or the rear I/O connection. This is also true for the SATA channels 0/1, which can either be used for an on-board SATA hard disk mezzanine module (C14-SATA) on the CD3-JIVE, or are externally available across J3. SATA channels 2/3 are also controlled by the BIOS, select either to be used externally on CompactPCI J3, or CompactPCI J5.

The COM1 port does not include the physical transceiver (TTL level only). This transceiver is located on the rear I/O module CDT-RIO instead. If COM1 is already in use on the CD3-JIVE by means of a PHY attached to P-CU or P-SA, the transceiver on the CDT-RIO must be inhibited by removing the CDT J-COM jumper.

Rear I/O is restricted to the J3 ... J5 connectors (except PXI across J2), hence the CD3-JIVE CPU card by default is suitable for any common 32/64-bit CompactPCI J1/J2 backplane.

Installing and Replacing Components

Before You Begin

Warnings

The procedures in this chapter assume familiarity with the general terminology associated with industrial electronics and with safety practices and regulatory compliance required for using and modifying electronic equipment. Disconnect the system from its power source and from any telecommunication links, networks or modems before performing any of the procedures described in this chapter. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage. Some parts of the system can continue to operate even though the power switch is in its off state.

Caution

Electrostatic discharge (ESD) can damage components. Perform the procedures described in this chapter only at an ESD workstation. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis or board front panel. Store the board only in its original ESD protected packaging. Retain the original packaging (antistatic bag and antistatic box) in case of returning the board to EKF for rapair.

Installing the Board

Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system
- Remove the board packaging, be sure to touch the board only at the front panel
- Identify the related *CompactPCI* slot (peripheral slot for I/O boards, system slot for CPU boards, with the system slot typically most right or most left to the backplane)
- Insert card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels)
- A card with onboard connectors requires attachment of associated cabling now
- Lock the ejector lever, fix screws at the front panel (top/bottom)
- Retain original packaging in case of return

Removing the Board

Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system

- Identify the board, be sure to touch the board only at the front panel
- unfasten both front panel screws (top/bottom), unlock the ejector lever
- Remove any onboard cabling assembly
- Activate the ejector lever
- Remove the card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels)
- Store board in the original packaging, do not touch any components, hold the board at the front panel only

Warning

Do not expose the card to fire. Battery cells and other components could explode and cause personal injury.

EMC Recommendations

CE

In order to comply with the CE regulations for EMC, it is mandatory to observe the following rules:

- The chassis or rack including other boards in use must comply entirely with CE
- Close all board slots not in use with a blind front panel
- Front panels must be fastened by built-in screws
- Cover any unused front panel mounted connector with a shielding cap
- External communications cable assemblies must be shielded (shield connected only at one end of the cable)
- Use ferrite beads for cabling wherever appropriate
- Some connectors may require additional isolating parts

Reccomended Accessories

Blind CPCI Front Panels	EKF Elektronik	Widths currently available (1HP=5.08mm): with handle 4HP/8HP without handle 2HP/4HP/8HP/10HP/12HP
Ferrit Bead Filters	ARP Datacom, 63115 Dietzenbach	Ordering No. 102 820 (cable diameter 6.5mm) 102 821 (cable diameter 10.0mm) 102 822 (cable diameter 13.0mm)
Metal Shielding Caps	Conec-Polytronic, 59557 Lippstadt	Ordering No. CDFA 09 165 X 13129 X (DB9) CDSFA 15 165 X 12979 X (DB15) CDSFA 25 165 X 12989 X (DB25)

Installing or Replacing the Memory Modules

Note: If you decide to replace the memory, observe the precautions in 'Before You Begin'

By default, the CD3-JIVE comes fully equipped and tested with two DDR2 SD-RAM memory modules. So normally there should be no need to install the memory modules.

The CD3-JIVE requires at least one PC2-3200/4200 (400/533MHz) DDR2 SDRAM SO-DIMM module, for better performance two SO-DIMMs of equal capacity are recommended. Further it is highly recommended that Serial Presence Detect (SPD) SO-DIMMs be used, since this allows the chipset to accurately configure the memory settings for optimum performance.

A replacement memory module must match the 200-pin SO-DIMM form factor (known from Notebook PCs), DDR2, V_{CC}=1.8V, PC2-3200/PC2-4200 (400/533MHz), on-die termination (ODT), unbuffered, non-ECC style. Suitable modules are available up to 1GB. The i915GM supports modules of up to a maximum of 14 address lines (A0...A13). Memory modules organized by more than14 address lines are not suitable.

Replacement of the Battery

When your system is turned off, a battery maintains the voltage to run the time-of-day clock and to keep the values in the CMOS RAM. The battery should last during the lifetime of the CD3-JIVE. For replacement, the old battery must be desoldered, and the new one soldered. It is recommended that you send back the board to EKF for battery replacement.

Warning

Danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type. Do not expose a battery to fire.

Technical Reference

Local PCI Devices

The following table shows the on-board PCI devices and their location within the PCI configuration space. These devices consist of the Ethernet controllers and several devices within the i915GM chip set.

Bus Number	Device Number	Function Number	Vendor ID	Device ID	Description
0	0	0	0x8086	0x2590	Host Bridge
0	2	0	0x8086	0x2592	Internal Graphics Device
0	2	1	0x8086	0x2792	Int. Graphics Config. Regs.
0	27	0	0x8086	0x2668	Intel High Definition Audio
0	28	0	0x8086	0x2660	PCI Express Port 1
0	28	1	0x8086	0x2662	PCI Express Port 2
0	28	2	0x8086	0x2664	PCI Express Port 3
0	28	3	0x8086	0x2666	PCI Express Port 4
0	29	0	0x8086	0x2658	USB UHCI Controller #1
0	29	1	0x8086	0x2659	USB UHCI Controller #2
0	29	2	0x8086	0x265A	USB UHCI Controller #3
0	29	3	0x8086	0x265B	USB UHCI Controller #4
0	29	7	0x8086	0x265C	USB 2.0 EHCI Controller
0	30	0	0x8086	0x244E	PCI-to-PCI Bridge
0	30	2	0x8086	0x266E	AC'97 Audio Controller
0	30	3	0x8086	0x266D	AC'97 Modem Controller
0	31	0	0x8086	0x2640	LPC Bridge
0	31	1	0x8086	0x266F	IDE Controller
0	31	2	0x8086	0x2651	SATA Controller
0	31	3	0x8086	0x266A	SMB Controller
3 [1]	0	0	0x8086	0x108B [2] 0x109A [2]	Ethernet Controller NC1
4 [1]	0	0	0x8086	0x108B [2] 0x109A [2]	Ethernet Controller NC2
5 [1]	0	0	0x8086	0x108B [2] 0x109A [2]	Ethernet Controller NC3
6 [1]	0	0	0x10B5	0x8111	PCIE to PCI Bridge

[1] This bus number can vary depending on the PCI enumeration schema implemented in BIOS.

[2] The CD3-JIVE is available with a 82573E (0x108B) or 82573L (0x109A) Ethernet controller.

Local SMB Devices

The CD3-JIVE contains a few devices that are reachable via the System Management Bus (SMBus). These are the clock generation chip, the SPD EEPROMs on the SO-DIMM memory modules, a general purpose serial EEPROM and a supply voltage and CPU temperature controlling device in particular. Other devices could be connected to the SMB via the *CompactPCI* signals IPMB SCL (J1 B17) and IPMB SDA (J1 C17).

Address	Description
0x58	Hardware Monitor/CPU Temperature Sensor (LM87)
0xA0	SPD of SODIMM1
0xA2	SPD of SODIMM2
0xAE	General Purpose EEPROM
0xD2	Main Clock Generation (CK-410M)

Hardware Monitor LM87

Located on the SMBus the CD3-JIVE offers a hardware monitor of type LM87/NSC. This device is capable to observe board and CPU temperatures as well as several supply voltages generated on the board with a resolution of 8 bit. The following table shows the mapping of the voltage inputs of the LM87 to the corresponding supply voltages of the CD3-JIVE:

Input	Source	Resolution [mV]	Register
AIN1	CPU Core Voltage	9.8	0x28
AIN2	+1.05V	9.8	0x29
VCCP1	+1.5V	14.1	0x21
VCCP2/D2-	+1.8V	14.1	0x25
+2.5V/D2+	+2.5V	13	0x20
+3.3V	+3.3V	17.2	0x22
+5V	+5V	26	0x23
+12V	+12V [1)]	62.5	0x24

[1)] Revision 1 or higher.

Beside the continuous measuring of temperatures and voltages the LM87 may compare these values against programmable upper and lower boundaries. As soon as a measurement violates the allowed value, the LM87 may request an interrupt via the GPI[11] of the ICH6.

GPIO Usage

GPIO Usage ICH6

CD3-JIVE GPIO Usage ICH6				
GPIO	Type	Tol.	Function	Description
GPI 0	I	5V	CPCI_REQ6#	CompactPCI Bus Request Line #6
GPI 1	I	5V	CPCI_REQ5#	CompactPCI Bus Request Line #5
GPI 2	I	5V	CPCI_INTP	CompactPCI Interrupt Request Line INTP
GPI 3	I	5V	CPCI_ENUM#	CompactPCI System Enumeration Line ENUM#
GPI 4	I	5V	CPCI_FAL#	CompactPCI Power Failure Line FAL#
GPI 5	I	5V	CPCI_DEG#	CompactPCI Power Degeneration Line DEG#
GPI 6	I	3.3V	GP_JUMP#	BIOS CMOS Values Reset Jumper J-GP
GPI 7	I	3.3V	CPCI_SYSEN#	CompactPCI System Slot Enable Line SYSEN#
GPI 8	I	3.3V	N/A	Not used on CD3 (fixed to GND)
GPI 9	I	3.3V	USB_OC4#	USB Port #4 Overcurrent Detect Line
GPI 10	I	3.3V	USB_OC5#	USB Port #5 Overcurrent Detect Line
GPI 11	I	3.3V	HM_INT#	Hardware Monitor LM87 Interrupt Line
GPI 12	I	3.3V	EXP_PME#	Expansion Interface PME# Line
GPI 13	I	3.3V	EXP_SMI#	Expansion Interface SMI# Line
GPI 14	I	3.3V	USB_OC6#	USB Port #6 Overcurrent Detect Line
GPI 15	I	3.3V	USB_OC7#	USB Port #7 Overcurrent Detect Line
GPO 16	O	3.3V	CPCI_GNT6#	CompactPCI Bus Grant Line #6
GPO 17	O	3.3V	CPCI_GNT5#	CompactPCI Bus Grant Line #5
GPO 18	O	3.3V	GP_LED	General Purpose LED Control (via PLD)
GPO 19	O	3.3V	ETH_Switch	Ethernet Switch (Front/Rear) LOW: Ethernet Port #1 via Rear I/O HIGH: Ethernet Port #1 via Front I/O
GPO 20	O	3.3V	PLD_SCL	Local Option Reg Interface (within PLD)
GPO 21	O	3.3V	PLD_SDA	Local Option Reg Interface (within PLD)
GPO 23	O	3.3V	CPCI_INTS_EN	Connect SERIRQ to CompactPCI Line INTS LOW: SERIRQ disconnected from INTS HIGH: SERIRQ connected to INTS
GPIO 24	O	3.3V	CPCI_SMB_EN	Connect CPCI IPMB to local SMBus LOW: IPMB disconnected from SMBus HIGH: IPMB connected to SMBus
GPIO 25	O	3.3V	CPCI_CLK_EN	Enable CompactPCI Clock Buffer
GPI 26	I	3.3V	N/A	Not used on CD3 (fixed to GND)

CD3-JIVE GPIO Usage ICH6				
GPIO	Type	Tol.	Function	Description
GPIO 27	O	3.3V	VGA_SWITCH	VGA Switching Line: LOW: VGA via Rear I/O HIGH: VGA via Front I/O
GPIO 28	I/O	3.3V	EJECT_LED	CPCI Hot Swap Ejector
GPI 29-31	I	3.3V	BOARD_CFG	Board Configuration Jumpers
GPIO 32	O	3.3V	NC1_EN	Enable Ethernet Controller NC1
GPIO 33	O	3.3V	NC2_EN	Enable Ethernet Controller NC2
GPIO 34	O	3.3V	NC3_EN	Enable Ethernet Controller NC3
GPI 40	I	5V	CPCI_REQ4#	CompactPCI Bus Request Line #4
GPI 41	I	3.3V	LPC_DRQEXP#	Expansion Interface LPC DMA Request Line
GPO 48	O	3.3V	CPCI_GNT4#	CompactPCI Bus Grant Line #4
GPO 49	OD	1.05V	CPU_PWRGD	CPU Power Good Line

GPIO Usage FWH

CD3-JIVE GPIO Usage FWH				
GPIO	Type	Tol.	Function	Description
GPI 0	I	3.3V	FWH_ID	FWH Identity: Fixed to GND (indicates FWH #1)
GPI 1	I	3.3V	IDE_CLBID#	IDE 80pol. Cable Detection Line
GPI 2	I	3.3V	WDOGRST	Last Hardware Reset caused by watchdog
GPI 3	I	3.3V	LSB PCB REV	GPI 4 GPI 3 Rev. 0 0 0 0 1 1 1 0 2 1 1 3+
GPI 4	I	3.3V	MSB PCB REV	

GPIO Usage SIO

CD3-JIVE GPIO Usage SIO				
GPIO	Type	Tol.	Function	Description
GPIO 13	I	5V [1)]	CPCI_64EN#	CompactPCI 64-Bit Backplane
GPIO 14	O	5V/8mA [1)]	SATA_SWITCH	Serial ATA Switch LOW: C14-SATA HIGH: CDT-RIO
GPIO 15	O	5V/8mA [1)]	TRSHDN	COM (Onboard) Enable/Disable LOW: Disable HIGH:Enable
GPIO 16	I/O	5V/24mA [1)]	SIO_GPIO16	GPIO on Expansion Interface P-EXP Pin 29
GPIO 17	I/O	5V/24mA [1)]	SIO_GPIO17	GPIO on Expansion Interface P-EXP Pin 30
GPIO 20	I/O	5V/8mA [1)]	PXI_TRIG0	PXI Trigger 0 on CompactPCI J2 Pin B16
GPIO 21	I/O	5V/8mA [1)]	PXI_TRIG1	PXI Trigger 1 on CompactPCI J2 Pin A16
GPIO 22	I/O	5V/24mA [1)]	SIO_GPIO22	GPIO J4 b23
GPIO 23	I/O	5V/24mA [1)]	SIO_GPIO23	GPIO J4 b22
GPIO 24	I/O	5V/24mA [1)]	SIO_GPIO24	GPIO J4 c25
GPIO 25	I/O	5V/24mA [1)]	SIO_GPIO25	Serial ATA Switch2 * LOW: CompactPCI J5 HIGH: CompactPCI J3 * Stuffing option: GPIO J4 c24
GPIO 26	I/O	5V/24mA [1)]	PXI_TRIG6	PXI Trigger 6 on CompactPCI J2 Pin E18
GPIO 27	I/O	5V/24mA [1)]	PXI_TRIG7	PXI Trigger 7 on CompactPCI J2 Pin E16

[1)] These GPIOs have pullup resistors of approx. 50kΩ within the SIO.

Configuration Jumpers

Reset Jumper BIOS CMOS RAM Values (J-GP)

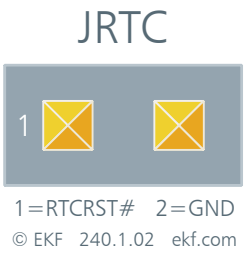
The jumper J-GP is used to bring the contents of the battery backed CMOS RAM to a default state. The BIOS uses the CMOS to store configuration values, e.g. the actual boot devices. Using this jumper is only necessary, if it is not possible to enter the setup of the BIOS. To reset the CMOS RAM mount a jumper on J-GP and perform a system reset. As long as the jumper is stuffed the BIOS will use the default CMOS values after any system reset. To get normal operation again, the jumper has to be removed.

J-GP	Function
Jumper OFF [1)]	No CMOS reset performed
Jumper ON	CMOS reset performed

[1)] This setting is the factory default.

Reset Jumper ICH6 RTC Core (J-RTC)

The jumper J-RTC is used to reset the battery backed core of the ICH6. This effects some registers within the ICH6 RTC core that are important before the CPU starts its work after a system reset. Note that J-RTC will neither perform the clearing of the CMOS RAM values nor resets the real time clock. To reset the RTC core the board must be removed from the system rack. Short-circuit the pins of J-RTC for about 1 sec. After that reinstall the board to the system and switch on the power. It is important to accomplish the RTC reset while the board has no power.



J-RTC	Function
Jumper OFF [1)]	No RTC reset performed
Jumper ON	RTC reset performed

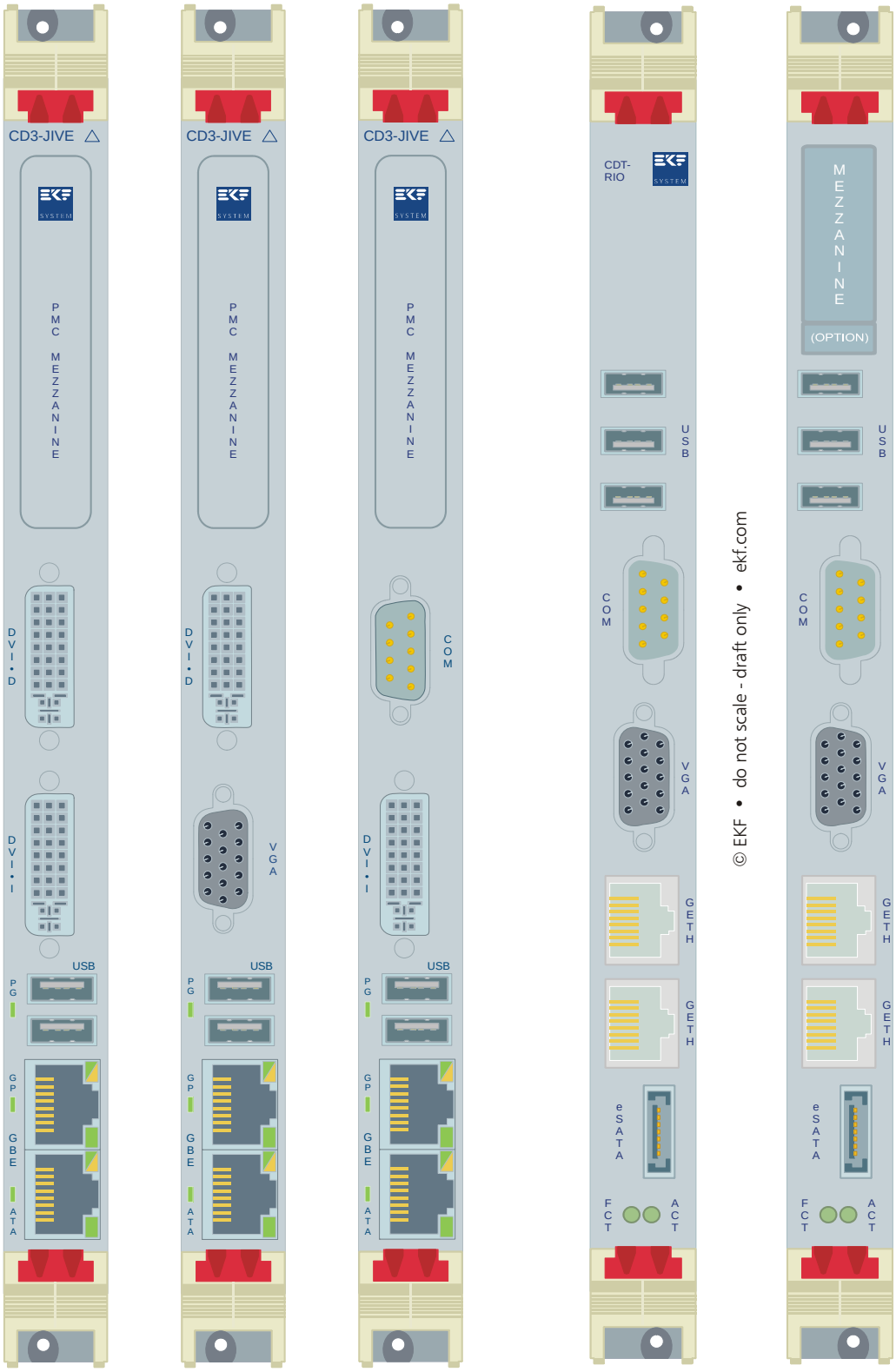
[1)] This setting is the factory default.

Connectors

Caution

Some of the internal connectors provide operating voltage (3.3V and 5V) to devices inside the system chassis, such as internal peripherals. Not all of these connectors are overcurrent protected. Do not use these internal connectors for powering devices external to the computer chassis. A fault in the load presented by the external devices could cause damage to the board, the interconnecting cable and the external devices themselves.

Front Panel CD3-JIVE / Back Panel CDT-RIO



CD3-JIVE
2 x DVI

CD3-JIVE
DVI & VGA

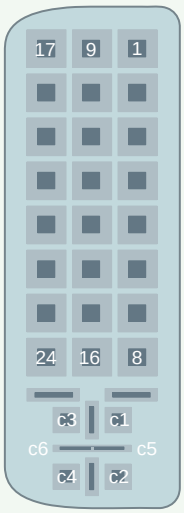
CD3-JIVE
DVI & COM

CDT-RIO
Standard
© EKF
ekf.com

CDT-RIO
Mezzanine
© EKF
ekf.com

CD3-JIVE Front Panel Elements
CDT-RIO Back Panel Elements

Video Monitor Connector DVI 1 (DVI-I)



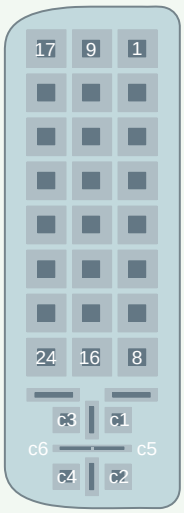
DVI 1 (DVI-I)					
17	TX0-	9	TX1-	1	TX2-
18	TX0+	10	TX1+	2	TX2+
19	GND	11	GND	3	GND
20		12		4	
21		13		5	
22	GND	14	DDC_POW [1]	6	DDC_SCL [2]
23	TXC+	15	GND	7	DDC_SDA [2]
24	TXC-	16	DVI_HP	8	VSYNC [2]

c3	BLUE [2]	c1	RED [2]
c6	GND	c5	GND
c4	HSYNC [2]	c2	GREEN [2]

[1] +5V protoected by a PolySwitch Fuse 0.75A.
[2] This signal may be switched either to the front connector or to the rear I/O adapter CDT-RIO.

For attachment of an ordinary analog RGB monitor to the DVI-I receptacle, there are both adapters and also adapter cables available from DVI-I to the HD-SUB15 connector. Attachment of digital monitors (flat panel displays) should be done by means of a DVI to DVI cable (single link style cable is sufficient).

Video Monitor Connector DVI 2 (DVI-D)



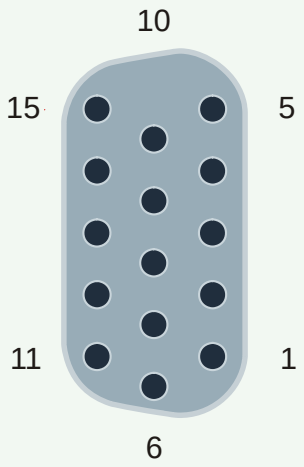
DVI 2 (DVI-D)					
17	TX0-	9	TX1-	1	TX2-
18	TX0+	10	TX1+	2	TX2+
19	GND	11	GND	3	GND
20		12		4	
21		13		5	
22	GND	14	DDC_POW [1]	6	DDC_SCL
23	TXC+	15	GND	7	DDC_SDA
24	TXC-	16	DVI_HP	8	

c3		c1	
c6	GND	c5	GND
c4		c2	

[1] +5V protoected by a PolySwitch Fuse 0.75A.

Video Monitor Connector VGA

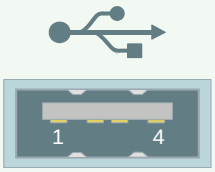
As an option, the CD3-JIVE can be equipped with a legacy VGA connector (High-Density D-Sub 15-position female connector). The VGA connector replaces the DVI 1 (DVI-I) receptacle, and the digital video interface therefore is not available with this option.



VGA (Option)	
1	RED [2]
2	GREEN [2]
3	BLUE [2]
4	NC
5	GND
6	GND
7	GND
8	GND
9	DDC_POW [1]
10	GND
11	NC
12	DDC_SDA [2]
13	HSYNC [2]
14	VSYNC [2]
15	DDC_SCL [2]

[1] +5V protoected by a PolySwitch Fuse 0.75A
[2] This signal may be switched either to the front connector or to the rear I/O adapter CDT-RIO.

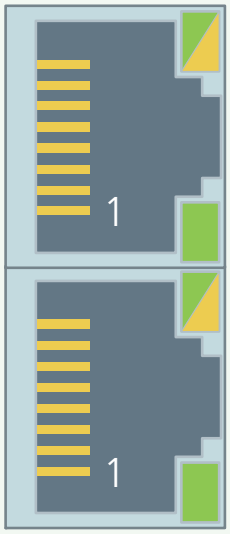
USB Connectors



[1] +5V protected by an Electronic Fuse 0.5A

USB Ports 1/2	
1	POW [1]
2	USB DATA NEG
3	USB DATA POS
4	GND

Ethernet Connectors

G-ETH1/2 (RJ45)		
 270.02.08.5	1	NC1_MDX0+ [1]
	2	NC1_MDX0- [1]
	3	NC1_MDX1+ [1]
	4	NC1_MDX2+ [1]
	5	NC1_MDX2- [1]
	6	NC1_MDX1- [1]
	7	NC1_MDX3+ [1]
	8	NC1_MDX3- [1]
	1	NC2_MDX0+
	2	NC2_MDX0-
	3	NC2_MDX1+
	4	NC2_MDX2+
	5	NC2_MDX2-
	6	NC2_MDX1-
	7	NC2_MDX3+
	8	NC2_MDX3-

[1] This signal may be switched either to the front connector or to the rear I/O adapter CDT-RIO.

The upper green/yellow dual-LED signals 1Gbit/s when lit yellow, 100Mbit/s when lit green, and 10Mbit/s when off. The lower green LED indicates LINK established when continuously on, and data transfer (activity) when blinking. If the lower green LED is permanently off, no LINK is established.

Available as an option, a 3rd GE F/P jack can be assembled together with a 8HP front panel (C24-GBE Mezzanine Module).

CD3-JIVE with 3rd Gigabit Ethernet Front Panel Jack Option

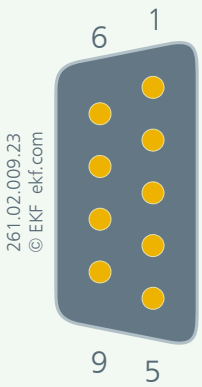
COM Port Connector

As an option, the CD3-JIVE can be equipped with a COM port connector (serial interface RS-232). The serial port connector is exclusive to the secondary video output connector DVI-D, due to limited space in the front panel.

The serial port interface is provided by the on-board SIO (Super I/O chip). As RS-232 line drivers/receivers, an ADM211E was chosen, featuring 230kbps guaranteed data rate. In order to enable the ADM211E, the jumper J-COM must be set (or a 0-Ohm shunt resistor position must be filled, in parallel to J-COM, as an alternative).

The serial connector COM should not be used concurrently with neither P-CU (on-board header for attachment of CU-series PHY modules), nor P-SA (SA modules), in order to avoid interference between signals from different sources. Hence, if either P-CU or P-SA is engaged, please remove jumper J-COM, which forces the ADM211E into its shutdown mode.

COM RS-232 (EIA/TIA 232) • Male D-Sub 9 • 261.02.009.23

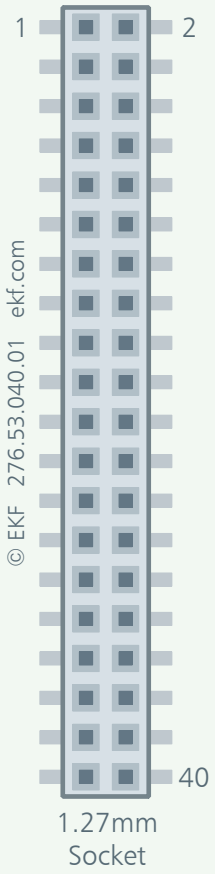


		1	DCD
DSR	6		
		2	RXD
RTS	7		
		3	TXD
CTS	8		
		4	DTR
RI	9		
		5	GND

Stuffing of connectors and other components described on this page are highly custom specific. Please discuss your actual needs with EKF (sales@ekf.de) before ordering.

Internal Connectors

Expansion Interface Header P-EXP



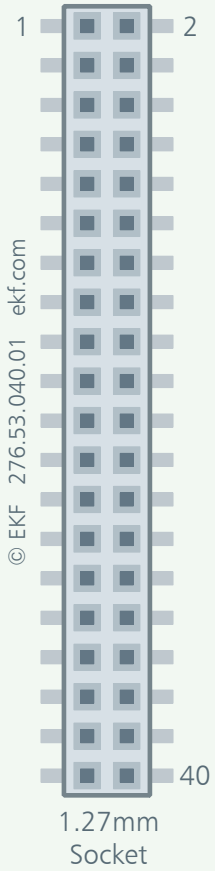
P-EXPT/P-EXPB			
GND	1	2	+3.3V
PCI_CLK	3	4	PCI_RST#
LPC_AD0	5	6	LPC_AD1
LPC_AD2	7	8	LPC_AD3
LPC_FRM#	9	10	LPC_DRQ#
GND	11	12	+3.3V
SERIRQ	13	14	EXP_PME#
EXP_SMI#	15	16	SIO_CLK14
FWH_ID0	17	18	FWH_INIT#
ICH_RCIN#	19	20	ICH_A20GATE
GND	21	22	+5V
USB_EXP_P2-	23	24	USB_EXP_P1-
USB_EXP_P2+	25	26	USB_EXP_P1+
USB_EXP_OC#	27	28	H_DBRESET#
SIO_GPIO16	29	30	SIO_GPIO17
GND	31	32	+5V
AC97_SDOUT	33	34	AC97_SDIN0
AC97_RST#	35	36	AC97_SYNC
AC97_BITCLK	37	38	AC97_SDIN1
SPEAKER	39	40	+12V/+VCCRTC [1)]

[1)] This pin is connected to+VCCRTC, alternatively it connects to +12V via a 0-Ohm jumper.

The expansion interface header is available on both sides of the board, top and bottom, in order to provide attachment of the CCA-LAMBADA either to the left or to the right side of the CD3-JIVE.

WARNING: Neither the +3.3V pin, nor the +5V pin, nor the +12V pin are protected against a short circuit situation! This connector therefore should be used only for attachment of an expansion board like CCA-LAMBADA. The maximum current flowing across these pins should be limited to 2A per power rail.

ATA/IDE Header P-IDE



P-IDET/P-IDEB			
IDE_RST#	1	2	GND
IDE_D07	3	4	IDE_D08
IDE_D06	5	6	IDE_D09
IDE_D05	7	8	IDE_D10
IDE_D04	9	10	IDE_D11
IDE_D03	11	12	IDE_D12
IDE_D02	13	14	IDE_D13
IDE_D01	15	16	IDE_D14
IDE_D00	17	18	IDE_D15
GND	19	20	+3.3V
IDE_DREQ	21	22	+3.3V
IDE_IOW#	23	24	GND
IDE_IOR#	25	26	GND
IDE_IORDY	27	28	+5V
IDE_DACK#	29	30	+5V
IDE_IRQ (INT 15)	31	32	GND
IDE_A1	33	34	IDE_CBLID#
IDE_A0	35	36	IDE_A2
IDE_CS1#	37	38	IDE_CS3#
IDE_ACT#	39	40	GND

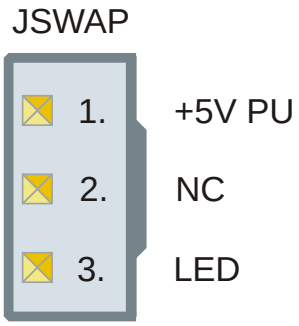
Like the expansion interface header the IDE connector is also available on both sides of the board.

WARNING: Neither the +3.3V pin, nor the +5V pin are protected against a short circuit situation! This connector therefore should be used only for attachment of the C10-CFA adapter or an expansion board like CCA-LAMBADA. The maximum current flowing across these pins should be limited to 2A per power rail.

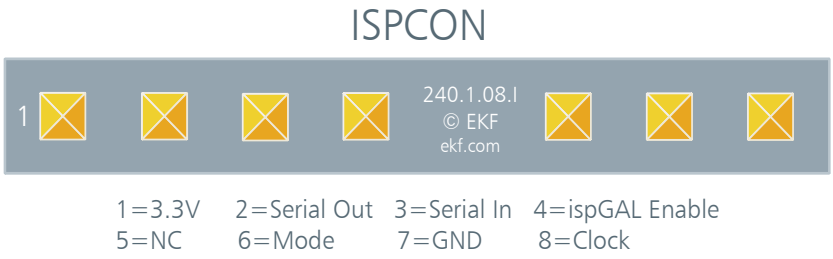
Speaker Header J-SPK

WARNING: The +5V pin is protected against a short circuit situation by a 0.1A PolySwitch. The JSPK connector should be used exclusively for direct attachment of a dynamic speaker device. When connecting to the input of a sound card, most likely a short-circuit situation will occur between the +5V pin of the JSPK connector and the GND pin of the audio-card input, which could cause permanent damage to the CD3-JIVE and the audio board, despite the PolySwitch resettable fuse. A workaround to this would be to place a 1k resistor across pin 1 and pin 2 of the JSPK connector, and strapping a single wire cable from JSPK pin 2 to the audio input.

Hot Swap Micro Switch Pin Row JSWAP



PLD Programming Header ISPCON



Note: The ISPCON is not stuffed. Its footprint is situated at the bottom side of the board.

Processor Debug Header P-ITP

P-ITP	
1	TDI
2	TMS
3	TRST#
4	NC
5	TCK
6	NC
7	TDO
8	BCLKN
9	BCLKP
10	GND
11	FBO
12	RST#
13	BPM5#
14	GND
15	BPM4#
16	GND
17	BPM3#
18	GND
19	BPM2#
20	GND
21	BPM1#
22	GND
23	BPM0#
24	DBA#
25	DBR#
26	VTAP
27	V_{TT}
28	V_{TT}

Note: The Debug Header is situated at the bottom side of the board.

CompactPCI J1

#J1	A	B	C	D	E
25	5V	*REQ64#* [2]	ENUM# [1]	3.3V	5V
24	AD1	5V	V(I/O)	AD0	*ACK64#* [2]
23	3.3V	AD4	AD3	5V	AD2
22	AD7	GND	3.3V	AD6	AD5
21	3.3V	AD9	AD8	M66EN [3]	C/BE0#
20	AD12	GND	V(I/O)	AD11	AD10
19	3.3V	AD15	AD14	GND	AD13
18	SERR# [1]	GND	3.3V	PAR	C/BE1#
17	3.3V	IPMB SCL [4]	IPMB SDA [4]	GND	PERR# [1]
16	DEVSEL# [1]	GND	V(I/O)	STOP# [1]	LOCK# [1]
15	3.3V	FRAME# [1]	IRDY# [1]	BDSEL# [6]	TRDY# [1]
14					
13			KEY AREA		
12					
11	AD18	AD17	AD16	GND	C/BE2#
10	AD21	GND	3.3V	AD20	AD19
9	C/BE3#	*GND* [5]	AD23	GND	AD22
8	AD26	GND	V(I/O)	AD25	AD24
7	AD30	AD29	AD28	GND	AD27
6	REQ# [1]	GND	3.3V	CLK	AD31
5	*BRSVP1A5* [5]	*BRSVP1B5* [5]	RST#	GND	GNT#
4	IPMB PWR	GND	V(I/O)	INTP [1]	INTS [1]
3	INTA# [1]	INTB# [1]	INTC# [1]	5V	INTD# [1]
2	*TCK* [5]	5V	*TMS* [5]	*TDO* [5]	*TDI* [5]
1	5V	-12V	*TRST#* [5]	+12V	5V

pin positions printed italic/coloured brown: reserved by specification and not connected

[1] This pin is pulled up with 1kΩ to V(I/O). Other pull up resistor values (e.g. 2.7kΩ for V(I/O)=+3.3V) are available on request.
[2] This pin is not used on CD3-JIVE, but pulled up with 1kΩ to V(I/O). Other pull up resistor valus on request.
[3] This pin is fixed to GND on CD3-JIVE to force 33MHz operation since 66MHz operation is not supported.
[4] This pin is pulled up with 2.4k to J1 pin A4.
[5] This pin is not connected.
[6] This is a short pin providing the last connection on hot board insertion.

CompactPCI J2

#J2	A	B	C	D	E
22	*GA4* [5]	*GA3* [5]	*GA2* [5]	*GA1* [5]	*GA0* [5]
21	CLK6	GND	*RSV*	*RSV*	*RSV*
20	CLK5	GND	*RSV*	GND	*RSV*
19	GND	GND	*RSV*	*RSV*	*RSV*
18	*BRSVP2A18*	*BRSVP2B18*	*BRSVP2C18*	GND	PXI_TRIG6 [3] *BRSVP2E18*
17	*BRSVP2A17*	GND	PRST# [1]	REQ6# [1]	GNT6#
16	PXI_TRIG1 [3] *BRSVP2A16*	PXI_TRIG0 [3] *BRSVP2B16*	DEG# [1]	GND	PXI_TRIG7 [3] *BRSVP2E16*
15	*BRSVP2A15*	GND	FAL# [1]	REQ5# [1]	GNT5#
14	*AD35* [1]	*AD34* [1]	*AD33* [1]	GND	*AD32* [1]
13	*AD38* [1]	GND	V(I/O)	*AD37* [1]	*AD36* [1]
12	*AD42* [1]	*AD41* [1]	*AD40* [1]	GND	*AD39* [1]
11	*AD45* [1]	GND	V(I/O)	*AD44* [1]	*AD43* [1]
10	*AD49* [1]	*AD48* [1]	*AD47* [1]	GND	*AD46* [1]
9	*AD52* [1]	GND	V(I/O)	*AD51* [1]	*AD50* [1]
8	*AD56* [1]	*AD55* [1]	*AD54* [1]	GND	*AD53* [1]
7	*AD59* [1]	GND	V(I/O)	*AD58* [1]	*AD57* [1]
6	*AD63* [1]	*AD62* [1]	*AD61* [1]	GND	*AD60* [1]
5	*C/BE5#* [1]	GND (64EN#) [1]	V(I/O)	*C/BE4#* [1]	*PAR64* [1]
4	V(I/O)	*BRSVP2B4*	*C/BE7#* [1]	GND	*C/BE6#* [1]
3	CLK4	GND	GNT3#	REQ4# [1]	GNT4#
2	CLK2	CLK3	SYSEN# [7]	GNT2#	REQ3# [1]
1	CLK1	GND	REQ1# [1]	GNT1#	REQ2# [1]

pin positions printed italic/coloured brown: reserved by specification and not connected

Coloured green - these signals may be in use for GPIO on J4

[1] This pin is pulled up with 1kΩ to V(I/O). Other pull up resistor values (e.g. 2.7kΩ for V(I/O)=+3.3V) are available on request.

[3] This pin is pulled up with 10kΩ to +5V.

[5] This pin is not connected.

[7] This pin is pulled up with 10kΩ to +3.3V.

CompactPCI J3

#J3	A	B	C	D	E
19	GND	GND	GND	GND	GND
18	LPa_DA+	LPa_DA-	GND	LPa_DC+	LPa_DC-
17	LPa_DB+	LPa_DB-	GND	LPa_DD+	LPa_DD-
16	LPb_DA+	LPb_DA-	GND	LPb_DC+	LPb_DC-
15	LPb_DB+	LPb_DB-	GND	LPb_DD+	LPb_DD-
14	GND	GND	GND	GND	GND
13	NC	NC	NC	NC	NC
12	NC	NC	NC	NC	NC
11	NC	NC	NC	NC	NC
10	NC	NC	NC	NC	NC
9	GND *NC*	GND *NC*	GND *NC*	GND *NC*	GND *NC*
8	SATA_TX3- [3] *NC*	SATA_TX3+ [3] *NC*	GND *NC*	SATA_RX3- [3] NC	SATA_RX3+ [3] *NC*
7	GND *NC*	GND *NC*	+5V *NC*	GND *NC*	GND *NC*
6	SATA_TX2- [3] *NC*	SATA_TX2+ [3] *NC*	GND *NC*	SATA_RX2- [3] *NC*	SATA_RX2+ [3] *NC*
5	GND *NC*	GND *NC*	+5V *NC*	GND *NC*	GND *NC*
4	SATA_TX1- [1] *NC*	SATA_TX1+ [1] *NC*	GND *NC*	SATA_RX1- [1] *NC*	SATA_RX1+ [1] *NC*
3	GND *NC*	GND *NC*	+5V *NC*	GND *NC*	GND *NC*
2	SATA_TX0- [1] *NC*	SATA_TX0+ [1] *NC*	GND *NC*	SATA_RX0- [1] *NC*	SATA_RX0+ [1] *NC*
1	NC SATA_ACT# [2]	GND *NC*	GND *NC*	GND *NC*	GND *NC*

J3 is optional (concurrent to PICMG 2.16 backplane)

Signals orange/italic: Deviant usage on CD2/CDY

[1] Signals can be switched between J3/J5

[2] Default SATA Activity LED in Front Panel of CD3-JIVE

[3] Signals can be switched between J3/P-SATA

CompactPCI J4

#J4	A	B	C	D	E
25	MS_DATA	SIO_GPIO20	SIO_GPIO24	KB_DATA	USB P2+
24	MS_CLK	SIO_GPIO21	NC [2]	KB_CLK	USB P2-
23	GND	SIO_GPIO22	SIO_GPIO26	GND	USB P1+
22	COM2 RI#	SIO_GPIO23	SIO_GPIO27	+5V	USB P1-
21	COM RTS#	COM DSR#	COM CTS#	COM DCD#	USB OC1#
20	NC	+5V	COM TXD	COM RXD	COM DTR#
19	GND	GND	NC	USB OC2# *NC*	USB P3+ *NC*
18	NC	NC	+5V	GND	USB P3- *NC*
17	+3.3V	+3.3V	NC	NC	USB P4+ *NC*
16	+5V	+5V	NC	NC	USB P4- *NC*
15	GND	GND	GND	GND	GND
14					
13		KEY AREA			
12					
11	VGA_RED	VGA_GREEN	VGA_BLUE	VGA_VSYNC	VGA_HSYNC
10	GND	GND	GND	DDC_SDA [1]	DDC_SCL [1]
9	+5V	GND	GND	GND	GND
8	+5V	GND	NC	GND	NC *IDE CBLID#*
7	+5V	NC *IDE CS1#*	GND	NC *IDE CS3#*	NC *IDE ACT#*
6	NC *IDE DACK#*	NC *IDE IRQ14*	NC *IDE A01*	NC *IDE A00*	NC *IDE A02*
5	GND	NC *IDE IOW#*	GND	NC *IDE IOR#*	NC *IDE IORDY*
4	NC *IDE D14*	NC *IDE D00*	NC *IDE D15*	GND	NC *IDE DREQ*
3	NC *IDE D03*	NC *IDE D12*	NC *IDE D02*	NC *IDE D13*	NC *IDE D01*
2	NC *IDE D09*	NC *IDE D05*	AC_SDIN0 *IDE D10*	AC_SDIN1 *IDE D04*	AC_SDIN2 *IDE D11*
1	AC_BITCLK *IDE RST#*	GND	AC_SYNC *IDE D07*	AC_SDOUT *IDE D08*	AC_RST# *IDE D06*

Signals orange/italic: Deviant usage on CD2/CDY

Coloured green - these signals may be in use for PXI trigger

[1] This pin is pulled up with 2.4kΩ to +4.3V.

[2] Stuffing option SIO_GPIO25

CompactPCI J5

#J5	A	B	C	D	E
22					
21	SATA0TN [1]	SATA0TP [1]	GND	SATA0RN [1]	SATA0RP [1]
20	NC	GND	+5V	GND	NC / *ACTLED#* [2]
19	SATA1TN [1]	SATA1TP [1]	GND	SATA1RN [1]	SATA1RP [1]
18					
17					
16	GND	GND	GND	GND	GND
15	GND	PMC1	PMC2	PMC3	PMC4
14	PMC5	PMC6	PMC7	PMC8	PMC9
13	PMC10	PMC11	PMC12	PMC13	PMC14
12	+3.3V	+3.3V	+3.3V	+5V	+5V
11	PMC15	PMC16	PMC17	PMC18	PMC19
10	PMC20	PMC21	PMC22	PMC23	PMC24
9	PMC25	PMC26	PMC27	PMC28	PMC29
8	PMC30	PMC31	PMC32	PMC33	PMC34
7	PMC35	PMC36	PMC37	PMC38	PMC39
6	PMC40	PMC41	PMC42	PMC43	PMC44
5	PMC45	PMC46	PMC47	PMC48	PMC49
4	PMC50	PMC51	PMC52	PMC53	PMC54
3	PMC55	PMC56	PMC57	PMC58	PMC59
2	PMC60	PMC61	PMC62	PMC63	PMC64
1	+3.3V	+3.3V	+3.3V	+5V	+5V

PMC signals derived from PMC mezzanine connector J4
[1] Signals can be switched between J3/J5
[2] Default SATA Activity LED in Front Panel of CD3-JIVE

P-CU Serial Interface Connectors

If the on-board RS-232 transceiver ADM211E is either not stuffed or disabled by removing the jumper JMP-COM, alternatively external PHY modules can be attached to the CD3-JIVE by means of a flat ribbon cable.

The CD3-JIVE may be equipped with the header P-CU, suitable for the EKF CU7/CU8 series of PHY modules. The CU7-RS485 is an isolated fieldbus interface, available either for party-line configuration or full-duplex point-to-point.

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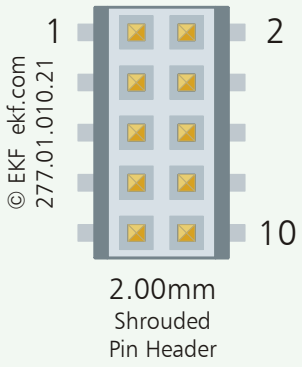
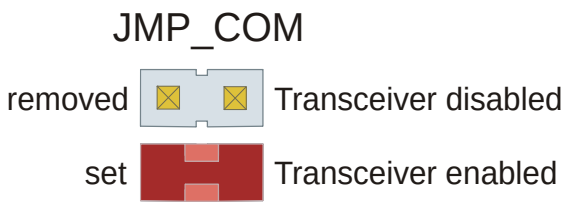
CU7-RS485

CU8-RS232

P-CU (2.00mm Pin Header 2 x 5)			
+5V/0.5A	1	2	DSR#
RI#	3	4	RXD
TXD	5	6	DTR#
RTS#	7	8	CTS#
DCD#	9	10	GND

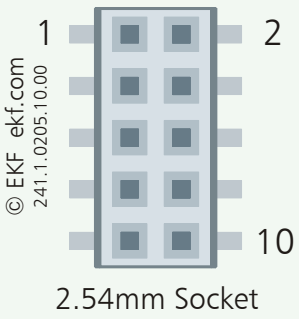




Remove JMP-COM to disable the on-board transceiver when using P-CU

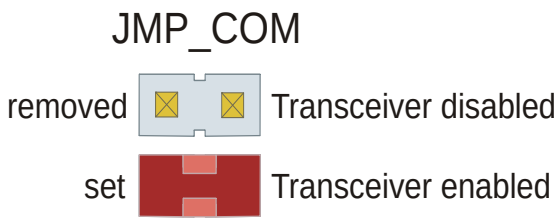
P-SA Serial Interface Connectors

Another header P-SA may be provided on the CD3-JIVE which complies with the MEN SA-series of PHY modules. No more than one transceiver may be in use, either P-CU, P-SA or the on-board transceiver



2.54mm Socket

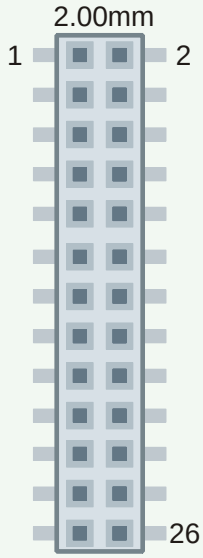
P-SA2 (2.54mm Socket 2 x 5)			
+5V/0.5A	2	1	GND
RXD	4	3	TXD
RTS#	6	5	DTR#
CTS#	8	7	DSR#
RI#	10	9	DCD#



Remove JMP-COM to disable the on-board transceiver when using P-SA

P-SATA

The CD3-JIVE can be optionally ordered with a 2.5-inch SATA hard disk mezzanine module (C14-SATA, single or dual drive). These signals can be switched between CompactPCI J3 and P-SATA



P-SATA (2.00mm Socket 2 x 13)				
	GND	1	2	GND
	SATA2TP	3	4	+5V
	SATA2TN	5	6	+5V
	GND	7	8	GND
	SATA2RN	9	10	+5V
	SATA2RP	11	12	+5V
	GND	13	14	GND
	SATA3TP	15	16	+3.3V
	SATA3TN	17	18	+3.3V
	GND	19	20	GND
	SATA3RN	21	22	+3.3V
	SATA3RP	23	24	+3.3V
	GND	25	26	GND

PMC Mezzanine MJ1

MJ1	Signal Name	Signal Name	MJ1
1	*TCK*	-12V	2
3	GND	INTA# [1)]	4
5	INTB# [1)]	INTC# [1)]	6
7	*BUSMODE1#*	+5V	8
9	INTD# [1)]	*Reserved*	10
11	GND	+3.3V (3.3Vaux)	12
13	CLK	GND	14
15	GND	GNT#	16
17	REQ#	+5V	18
19	VI/O [3)]	AD31	20
21	AD28	AD27	22
23	AD25	GND	24
25	GND	C/BE3#	26
27	AD22	AD21	28
29	AD19	+5V	30
31	VI/O [3)]	AD17	32
33	FRAME#	GND	34
35	GND	IRDY#	36
37	DEVSEL#	+5V	38
39	GND	LOCK#	40
41	*Reserved*	*Reserved*	42
43	PAR	GND	44
45	VI/O [3)]	AD15	46
47	AD12	AD11	48
49	AD09	+5V	50
51	GND	C/BE0#	52
53	AD06	AD05	54
55	AD04	GND	56
57	VI/O [3)]	AD03	58
59	AD02	AD01	60
61	AD00	+5V	62
63	GND	REQ64# [2)]	64

pin positions printed italic/coloured brown: reserved by specification and not connected
pin positions printed italic/coloured blue: not connected on CD3-JIVE

Notes:

[1)] This pin position is showing the actual interrupt assignment on the CD3-JIVE local PCI bus.
[2)] This pin position is pulled to +3.3V via separate 3.3 KΩ resistor.
[3)] $V_{I/O}$ is fixed to +3.3V on CD3-JIVE

PMC Mezzanine MJ2

MJ2	Signal Name	Signal Name	MJ2
1	+12V	*TRST#*	2
3	*TMS*	*TDO*	4
5	*TDI*	GND	6
7	GND	*Reserved*	8
9	SERIRQ [2)]	*Reserved*	10
11	BUSMODE2# [3)]	+3.3V	12
13	RST#	BUSMODE3# [4)]	14
15	+3.3V	BUSMODE4# [4)]	16
17	PME#	GND	18
19	AD30	AD29	20
21	GND	AD26	22
23	AD24	+3.3V	24
25	IDSEL [1)]	AD23	26
27	+3.3V	AD20	28
29	AD18	GND	30
31	AD16	C/BE2#	32
33	GND	*Reserved*	34
35	TRDY#	+3.3V	36
37	GND	STOP#	38
39	PERR#	GND	40
41	+3.3V	SERR#	42
43	C/BE1#	GND	44
45	AD14	AD13	46
47	M66EN	AD10	48
49	AD08	+3.3V	50
51	AD07	*Reserved*	52
53	+3.3V	*Reserved*	54
55	*Reserved*	GND	56
57	*Reserved*	*Reserved*	58
59	GND	*Reserved*	60
61	ACK64# [3)]	+3.3V	62
63	GND	*Reserved*	64

BUSMODE[4:2] signals coded according to P1386/Draft 2.4a pg. 48 (PCI protocol capable card)

pin positions printed italic/coloured brown: reserved by specification and not connected
pin positions printed italic/coloured blue: not connected on CD3-JIVE

Notes:
[1)] IDSEL is assigned to AD16.
[2)] This pin position is normally a PMC reserved pin, on CD2 it may be used to connect to the SERIRQ signal.
[3)] This pin position is pulled to +3.3V via separate 3.3 KΩ resistor.
[4)] This pin position is pulled to GND via separate 1.0 KΩ resistor.

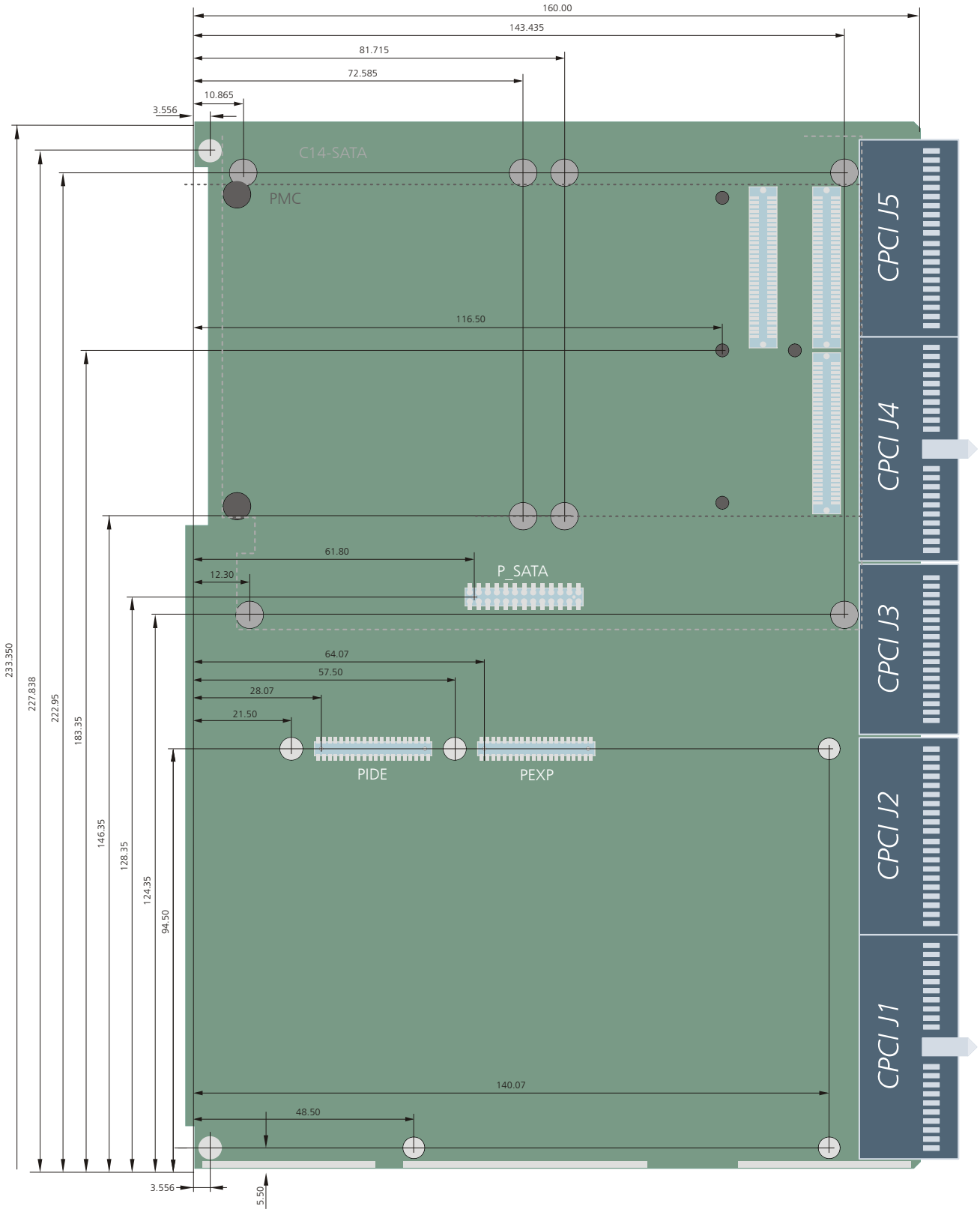
PMC Mezzanine MJ4

CompactPCI J5	MJ4	Signal Name	Signal Name	MJ4	*CompactPCI* J5
B15	1	I/O 01	I/O 02	2	C15
D15	3	I/O 03	I/O 04	4	E15
A14	5	I/O 05	I/O 06	6	B14
C14	7	I/O 07	I/O 08	8	D14
E14	9	I/O 09	I/O 10	10	A13
B13	11	I/O 11	I/O 12	12	C13
D13	13	I/O 13	I/O 14	14	E13
A11	15	I/O 15	I/O 16	16	B11
C11	17	I/O 17	I/O 18	18	D11
E11	19	I/O 19	I/O 20	20	A10
B10	21	I/O 21	I/O 22	22	C10
D10	23	I/O 23	I/O 24	24	E10
A9	25	I/O 25	I/O 26	26	B9
C9	27	I/O 27	I/O 28	28	D9
E9	29	I/O 29	I/O 30	30	A8
B8	31	I/O 31	I/O 32	32	C8
D8	33	I/O 33	I/O 34	34	E8
A7	35	I/O 35	I/O 36	36	B7
C7	37	I/O 37	I/O 38	38	D7
E7	39	I/O 39	I/O 40	40	A6
B6	41	I/O 41	I/O 42	42	C6
D6	43	I/O 43	I/O 44	44	E6
A5	45	I/O 45	I/O 46	46	B5
C5	47	I/O 47	I/O 48	48	D5
E5	49	I/O 49	I/O 50	50	A4
B4	51	I/O 51	I/O 52	52	C4
D4	53	I/O 53	I/O 54	54	E4
A3	55	I/O 55	I/O 56	56	B3
C3	57	I/O 57	I/O 58	58	D3
E3	59	I/O 59	I/O 60	60	A2
B2	61	I/O 61	I/O 62	62	C2
D2	63	I/O 63	I/O 64	64	E2

Appendix

Mechanical Drawings

The following drawing shows the positions of mounting holes and expansion connectors on the CD3-JIVE.



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